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EIA
STANDARD

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TP-109

LOOP INDUCTANCE MEASUREMENT TEST PROCEDURE FOR ELECTRICAL CONNECTORS
(1 nH – 10 nH)

EIA-364-109

May 2003

ELECTRONIC COMPONENTS, ASSEMBLIES & MATERIALS ASSOCIATION
THE ELECTRONIC COMPONENTS SECTOR OF THE ELECTRONIC INDUSTRIES ALLIANCE

NOTICE

This EIA Standard is considered to have International Standardization implication, but the International Electrotechnical Commission activity has not progressed to the point where a valid comparison between the EIA Standard and the IEC document can be made.

This Standard does not purport to address all safety problems associated with its use or all applicable regulatory requirements. It is the responsibility of the user of this Standard to establish appropriate safety and health practices and to determine the applicability of regulatory limitations before its use.

(From Standards Proposal No. 4831, formulated under the cognizance of the ECA CE-2.0 Committee on National Connector Standards.

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CONTENTS

Clause Page

Figure

TEST PROCEDURE No. 109

LOOP INDUCTANCE MEASUREMENT TEST PROCEDURE
FOR
ELECTRICAL CONNECTORS (1 nH – 10 nH)

(From EIA Standards Proposal No. 4831, formulated under the cognizance EIA CE-2.0 Committee on National Connector Standards.)

1 Introduction

1.1 Scope

This procedure applies to interconnect assemblies, such as electrical connectors and sockets.

1.2 Object

This standard describes a test method to measure the loop inductance (1 nH – 10 nH range) in the frequency domain using probes and vector network analyzer.

> NOTE — This test method is written for test professionals who are knowledgeable in the electronics field and are trained to use the referenced equipment. Because the measurement values are heavily influenced by the fixture and equipment this method cannot describe all of the possible combinations. The major equipment manufacturers provide Application Notes for more in-depth technical description of how to optimize the use of their equipment. It is imperative that the referencing document include the necessary description and sketches for the test professional to understand how to setup and perform the requested measurements.

1.3 Definitions

1.3.1 Specimen environment impedance

The impedance presented to the signal conductors by the fixture. This impedance is a result of transmission lines, termination resistors, attached receivers or signal sources, and fixture parasitics.

1.3.2 Inductance

The property of a circuit or circuit element that opposes a change in current flow. Inductance causes current changes to lag behind voltage changes. It is measured in Henrys.

1.3.3 Self inductance (L)

The inductance of a single conductor.

1.3.4 Mutual inductance (L_m)

The common property of two electric conductors whereby a voltage (electromotive force) is induced across one conductor by a change of current in the other conductor.

1.3.5 Loop inductance (L_{Loop})

The inductance of two or more conductors in which the current flows into one conductor and returns through the other(s). The loop is defined as the current path inscribed by the 'drive' and 'return' path in the conductors.

$$L_{Loop} = L_1 + L_2 - \left(2 * L_m\right)$$

where: L_1 = self inductance of the driven conductor
L_2 = self inductance of the return path conductor(s)
L_m = mutual inductance between the drive and return path conductors.

1.3.6 Mutual inductance coupling coefficient (K_m)

The measure of degree of magnetic coupling between two conductors. It is a unitless parameter and is defined as follows:

$$K_m = \frac{L_m}{\sqrt{L_1 * L_2}}$$

1.3.7 Inductive reactance

The resistance presented to an alternating current (ac) due to the inductance of a connector and is measured in ohms. It is also the imaginary term of the impedance and is directly proportional to the inductance and to the frequency of the applied voltage.

1.3.8 Termination (electronics usage)

An impedance connected to the end of a transmission line, typically to minimize reflected energy on the line.

2 Test resources

2.1 Equipment

A vector network analyzer shall be used. Microprobes, semi-rigid coax, or similar high frequency test hardware shall be used to minimize fixture influence on the measurement results. It is recommended that a precision x-y positioning station be used to prevent probe damage and provide precision, consistent probe placement. See annex A for sketches of the probes and test equipment set up.

NOTES

1 The test professional should be aware of the frequency limitations of the fixture.
2 The test professional should be aware of any limitations of any mathematical functions performed (e.g. normalization, inverse FFT, or software filtering.)

2.2 Fixture

The generic term “probe(s)” is used throughout the procedure to refer to semi-rigid coax, commercially available microprobes, or similar test hardware.

The “fixture” shall consist of either the probes alone or the probes in conjunction with a test board.

2.2.1 General

2.2.1.1 The fixture shall provide a low inductance path to the specimen. It is recommended that the fixture inductance be less than the specimen inductance. This can be aided by keeping the trace lengths as short as possible, and the traces as wide as possible.

2.2.1.2 The specimen may be probed directly or through a test board. It is recommended that the specimen be probed directly (without a test board) to minimize measurement error. Test boards, when used, shall provide pads such that the probes may contact the board. Measurement variations can be minimized by keeping the pads as small as possible as this will allow repeatable microprobe placement and more uniform pad thickness.

2.2.1.3 The fixture shall allow one signal line to be driven at a time. The fixture shall allow one or more return path conductors to be connected to the measuring equipment. The fixture(s) shall allow for enough measurements throughout the specimen such that variations in geometries, materials, transmission paths, etc. may be demonstrated and provide a representative sampling of specimen performance.

NOTE — The fixture geometry and materials will impact the measurements due to the fixture parasitics. Usually the product's intended use dictates the most meaningful way to fixture it.

2.2.1.4 The far end of the driven line should be terminated in a low inductance electrical short circuit to the return conductor(s). The short circuit may be achieved by using a copper block or by shorting together all contacts on the test board.

2.2.2 Specimen environment impedance

Unless otherwise specified in the referencing document, the specimen environment impedance shall match the impedance of the test equipment. Typically this will be 50 ohms.

2.2.3 Calibration features

NOTE — The term “calibration” used in this document is not to be confused with the periodic factory equipment calibration. Calibration is used in the sense of characterizing the fixture so that when the “fixture plus specimen” measurement is taken, the characteristics of the specimen alone can be accurately determined.

2.2.4.1 Equipment calibration standard

For calibration of the vector network analyzer, calibration standards shall be used to conduct the open, short, and load calibration. When probes are used the calibration shall be conducted such that the calibration plane is at the tip of the probes. For example a ceramic substrate with open, short, and load standards may be used.

NOTE — Other calibration techniques such as through-reflect-line may be used. The calibration standard and fixture shall incorporate features appropriate to the calibration method(s) being used.

2.2.4.2 Test board characterization structure

The test board, if used, shall provide a reference structure such that a loop inductance measurement can be conducted. This structure shall be identical to that used for the measurement of the specimen, except that a short circuit is included between the driven and return paths where the specimen would otherwise be located. It is recommended that a ground plane be used as the return path to provide the lowest possible inductance, to minimize the effect of the fixture on the measurement result. See annex C for a discussion of calibration and reference traces.

3 Test specimen

3.1 Description

For this test procedure the test specimen shall be as follows:

3.1.1 Connectors

A connector or mated connector pair.

3.1.2 Sockets

A socket and test device.

4 Test procedure

4.1 Set the vector network analyzer to measure S_{11} for loop inductance.

4.2 Calibrate the equipment and fixture according to the manufacturer's specifications using the calibration standard. The calibration plane is to be directly at the probe interface to the fixture; see 2.2.4.1 for more detailed information. Unless otherwise specified in the referencing document it is recommended that the following equipment settings be used:

- Smith chart format,
- set network analyzer to display inductance values,
- minimum of 401 measurement points,
- frequency span – conduct both wideband and narrowband sweeps,
- no smoothing,
- averaging set to 16 or higher.

NOTE — "Wideband" sweep is typically the full range of the network analyzer and "narrowband" sweep is over a limited range (for example 100 MHz wide).

4.3 Fixture measurement

Position the probes to touch the interface pads of the test board characterization structure. Measure and record the loop inductance of the fixture from the Smith chart at the frequency(s) of interest.

> NOTE — A loop inductance vs. frequency graph may be generated through the use of data acquisition software and spreadsheet software, if specified in the referencing document.

4.4 Specimen measurement

4.4.1 Connect the probe to the fixture interface pad of the driven line with the specimen installed as shown in figure A.1. Terminate the far end of the driven line in an electrical short circuit to the return conductor(s).

4.4.2 Place the specimen a minimum of 5 cm from any object that may introduce error into the measurement.

4.4.3 Measure and record the loop inductance over the specified test frequency range or discrete frequencies.

4.4.4 Calculate the specimen loop inductance by subtracting the fixture loop inductance, (see 4.3) from the specimen plus fixture loop inductance, see 4.4.3.

NOTE — If specified in the referencing document, a loop inductance vs. frequency graph may be generated through the use of data acquisition software and spreadsheet software.

4.4.5 If requested, repeat 4.4.1 through 4.4.4 on multiple conductors throughout the specimen.

4.4.6 When additional measurements with different test frequencies or ranges are required perform the calibration step defined in 4.2, then repeat 4.4.1 through 4.4.5 as necessary.

5 Details to be specified

The following details shall be specified in the referencing document:

5.1 Measurement frequency range and/or discrete frequency(s)

5.2 Special requirements with respect to the fixture, and the short circuit, (see 2.2.1.4) construction and electrical properties of each.

5.3 Signal/ground pattern, including the number and location of signal and grounds. It is recommended that enough locations within the specimen be measured to take into account the varying loop inductances within the specimen

5.4 Location of the drive signal connection point, location of the return signal connection point and connections to be made to adjacent pins, if any

5.5 Specimen environment impedance if other than 50 ohms

5.6 Plots, if desired, and Smith charts or loop inductance vs. frequency graphs

6 Test documentation

Documentation shall contain the details specified in clause 5, with any exceptions, and the following:

6.1 Title of test

6.2 Test equipment used, and date of last and next calibration

6.3 Description of test fixture and associated calibration structures

6.4 Values and observations

6.5 Representative graphs, if available

6.6 Name of operator and date of test

Annex

A Loop inductance measurement setup (normative)

A.1 Figure A.1 shows an example of a typical test equipment setup for loop inductance measurements including the equipment, cables, probes, and fixture.

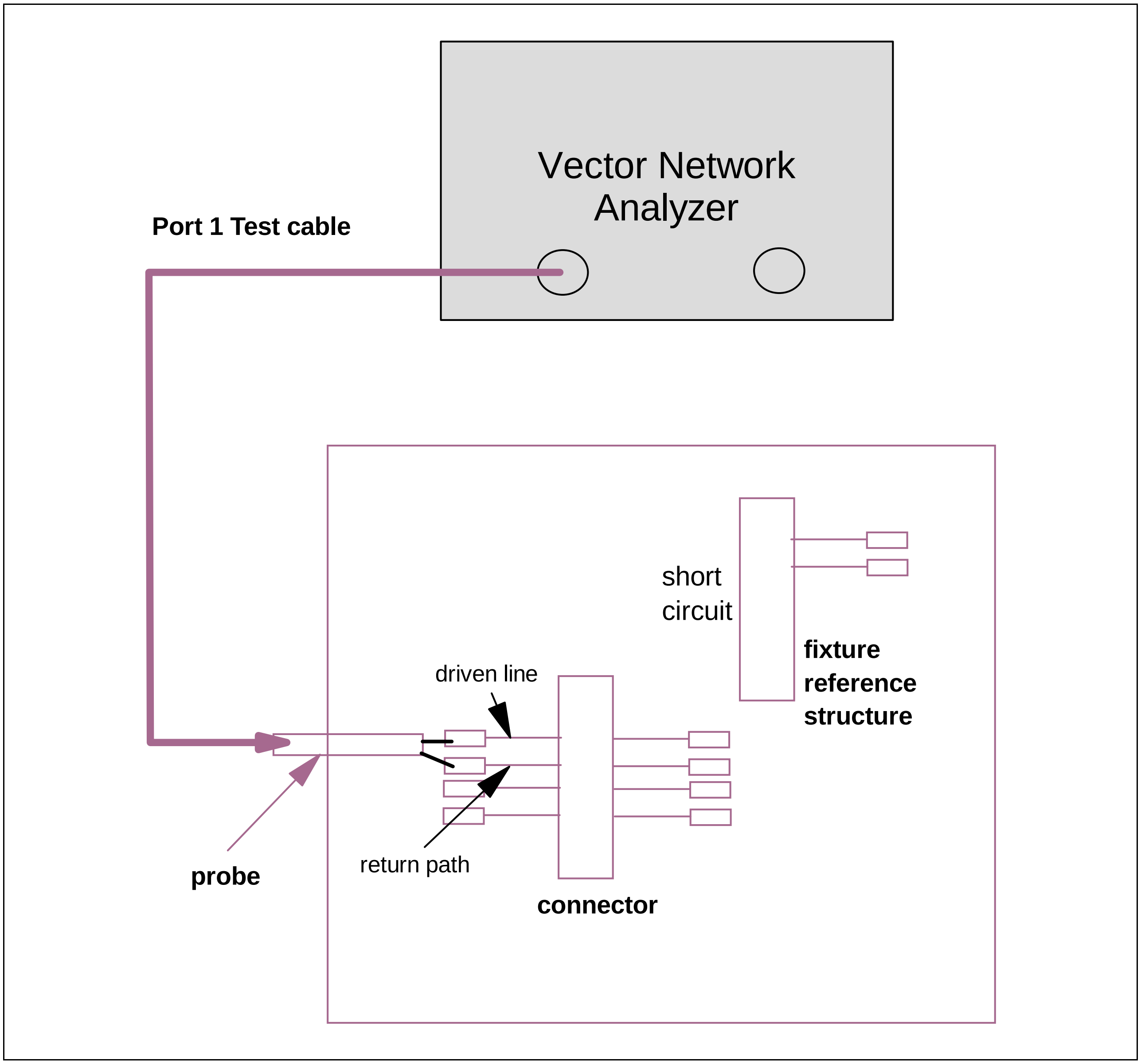

Figure A.1 - Example of test equipment setup for loop inductance measurements

A.2 Figure A.2 shows an example of the measurement set up for measuring the loop inductance of a fixture with a ground plane return path. The signal and ground vias are shorted together with a copper surface. The test fixture should be designed such that the signal trace, pad interface, and copper surface provide the lowest inductance path from the probe tip to the signal and ground vias. This reference trace and pad interface should represent the same structures and geometries that will be used for the specimen measurement.

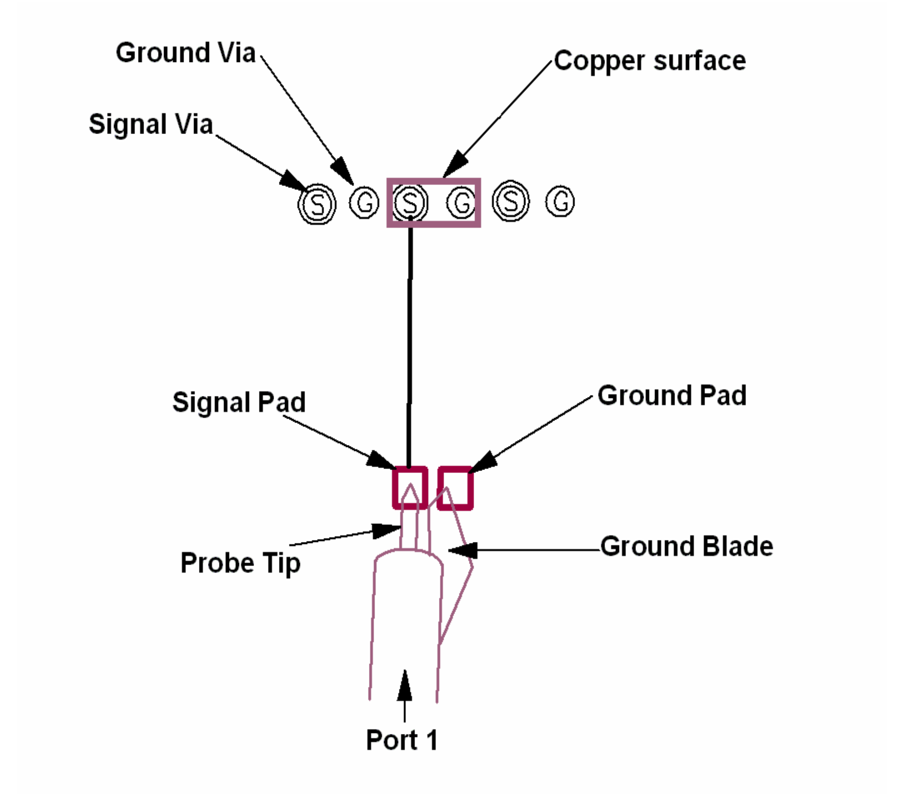

Figure A.2 - Example of fixture loop inductance measurement setup

A.3 Figure A.3 shows an example of the measurement set up for measuring the loop inductance of the fixture plus specimen. The figure shows an example of the probe, pads, shorting block, and a specimen consisting of an edgecard connector. The ground pad is connected to the test board ground plane (not shown) that is in turn connected to the specimen ground contacts. It is important that the shorting block connect the specified return path conductors, but not adjacent signal pins.

Figure A.3 - Example of loop inductance measurement setup

A.4 Figure A.4 shows a drawing of a microprobe contacting the bottom side of the PCB test fixture and the specimen mounted on the opposite side of the PCB. The test professional should be aware that this type of fixture may be used, but that all vias and traces should be taken into consideration when conducting the calibration procedures.

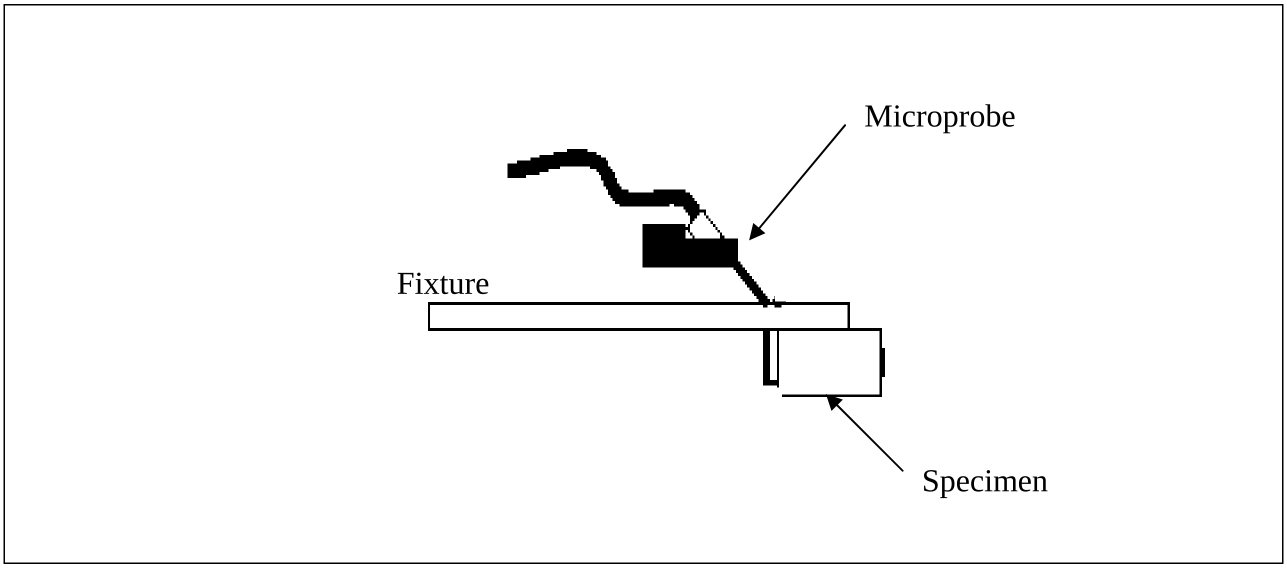

Figure A.4 - Diagram of microprobes contacting the bottom side of the printed circuit board test fixture

B Calibration standards and test board reference traces (informative)

B.1 Calibration standards

B.1.1 For the equipment calibration, a traceable calibration impedance standard should be used for a reference baseline. Specific equipment calibration should be performed according to the manufacturer's instructions. However, care should be taken as to what standards or other fixtures are used for the calibration procedure.

> NOTE — The term "calibration" used in this document is not to be confused with the periodic factory equipment calibration. Calibration is used in the sense of characterizing the fixture so that when the "fixture plus specimen" measurement is taken, the characteristics of the specimen alone can be accurately determined.

B.1.2 When possible the fixture should be designed to allow the attachment of the calibration standard as close to the specimen as possible. Reflections from fixture imperfections increase measurement error.

B.1.3 Printed circuit test boards should not be used as calibration standards. Because of different printed circuit board technologies, fabrication control, and material variations, it becomes difficult to insure that different board designs or fabrication techniques will have the same calibration reference for the impedance measurements. The impedance value of "controlled impedance traces" on a printed circuit board is typically ± 10% or ± 5% of the target value. In measurements and applications, this may be an acceptable tolerance to hold, however, for calibration purposes, this should not be used as a baseline.

B.1.4 The use of the traceable standard termination at the end of the test cable will allow the test fixture printed circuit board effects to be measured more accurately. The test professional will be able to accurately measure the impedance or transmission characteristic of the printed circuit board fixture, and not allow the test equipment to try to compensate for any fixture discontinuities.

B.1.5 Figures B.1 through B.4 show single ended test boards using SOLT (Short-Open-Load-Through) calibration trace structures. Calibration using other methods, for example TRL (Through-Reflect-Line), will require different structures.

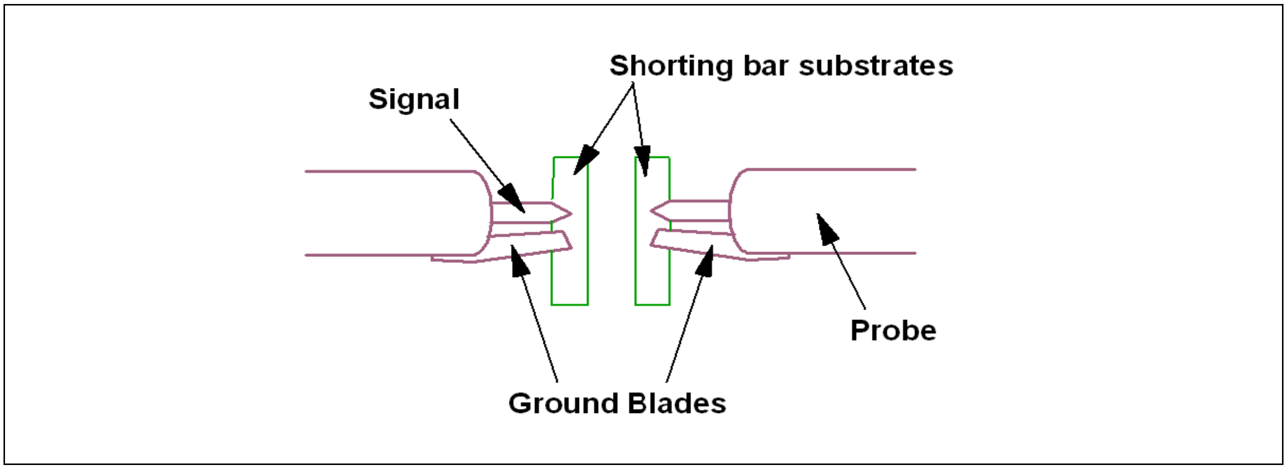

Figure B.1 – Short reference trace

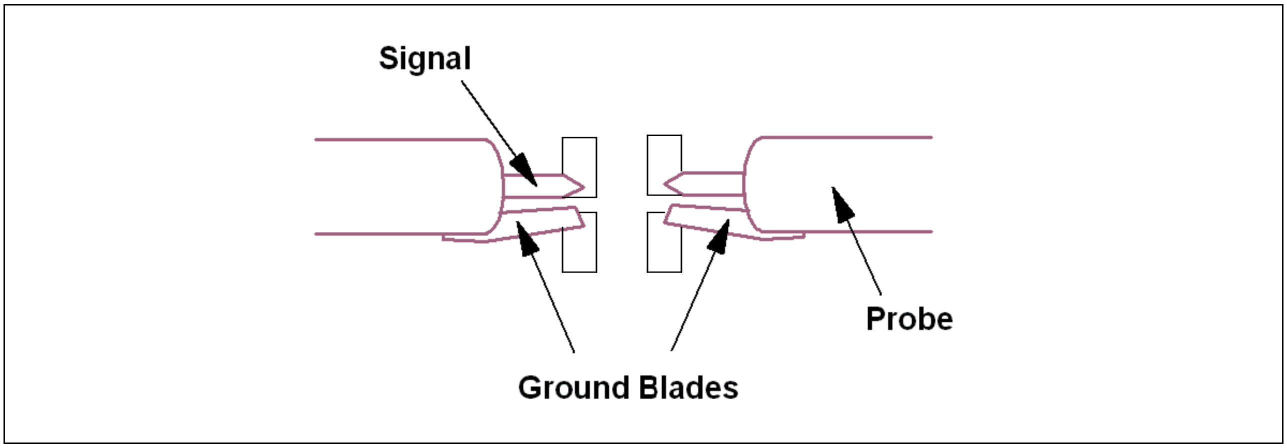

Figure B.2 – Open reference trace

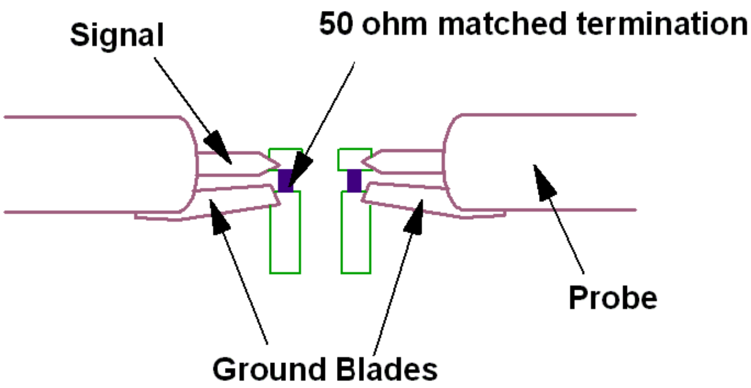

Figure B.3 – Fifty ohm load reference trace

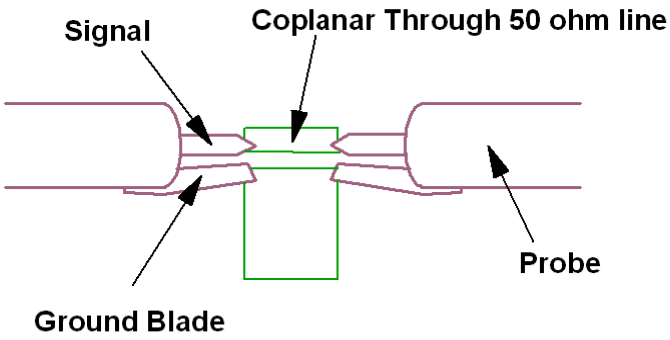

Figure B.4 – Transmission reference trace

B.2 Test board reference traces

Test boards shall include reference traces for measuring the frequency domain characteristics of the fixture in order to correct for fixture effects (e.g., discontinuities in impedance). Recommended test fixture configurations include:

B.2.1 A reference trace ending in a via which is shorted to the return path conductor(s). The length of this reference trace should be the same as that of the trace connected to the near end of the specimen.

B.2.2 A reference trace ending in a via which is open with respect to the return path conductor(s). The length of this reference trace should be the same as that of the trace connected to the near end of the specimen.

B.2.3 A reference trace terminated in the specimen environment impedance. The length of this reference trace should be the same as that of the trace connected to the near end of the specimen.

B.2.4 A reference structure consisting of a through transmission trace whose length is equal to the total fixture trace length for a single path, (length of the near end and far end traces). The test fixture shall provide an identical coaxial cable or probe connection at both ends.

NOTE 1 — This reference structure should be designed with the same configuration in which the specimen would be used in a typical application (such as footprint pads, grounds, traces, vias, etc).

NOTE 2 — The calibration structures above are described as terminating in a via. This is appropriate for pin-in-hole terminations, but is not appropriate for all terminations, e.g. surface mount connectors. Ideally the reference trace should terminate in the same type of pad or connection as the actual connector would experience.

C Printed circuit board design considerations for electronics measurements (informative)

This annex provides a general overview of circuit board design considerations for numerous electronics measurements, not just inductance. Although several clauses do not pertain to inductance measurements, the information is provided for the user who may design a single test board to perform multiple electronics measurements.

C.1 The designer should take precautions in designing printed-circuit boards for high-speed testing for several reasons. These include reflections due to impedance mismatches, signal attenuation due to skin effect of the narrow conductors, resonance effects due to long traces, crosstalk between traces, and others. Printed circuit board features that may be of concern include vias, SMT pads, probe interface, etc. Electrical discontinuities caused by these features are unavoidable in the test fixture(s), and shall not be overlooked as they may affect the impedance results of the specimen. This annex can not in the space allotted cover these topics in detail, but will attempt to lay the groundwork for further analysis and design, and refer the reader to more detailed treatments of the subject. There are a number of excellent references on the subject, which are listed at the end of this annex.

C.2 When the printed circuit board traces approach critical lengths (defined later in the document), it becomes essential to design the traces to match the impedance of the test equipment to avoid inaccurate results due to reflections. Controlling the line impedance of printed circuit board traces is difficult without the use of embedded reference planes in the board. The preferred reference plane is one connected to signal ground, but any low impedance reference will work (including a voltage plane) if it is sufficiently decoupled. The signal line impedance is determined by conductor geometry, including the trace width and thickness, distance from the ground or other reference plane or conductor, and the dielectric constant of the board material. In the case of differential trace pairs, the spacing between the two traces is also critical. Several formulas exist for calculation of printed circuit board trace impedance, and a number of impedance calculation software tools are also available. The choice of board impedance formula is based on the conductors' relative placement as well as their position in the board cross-section, some common examples of which are shown in the figures below.

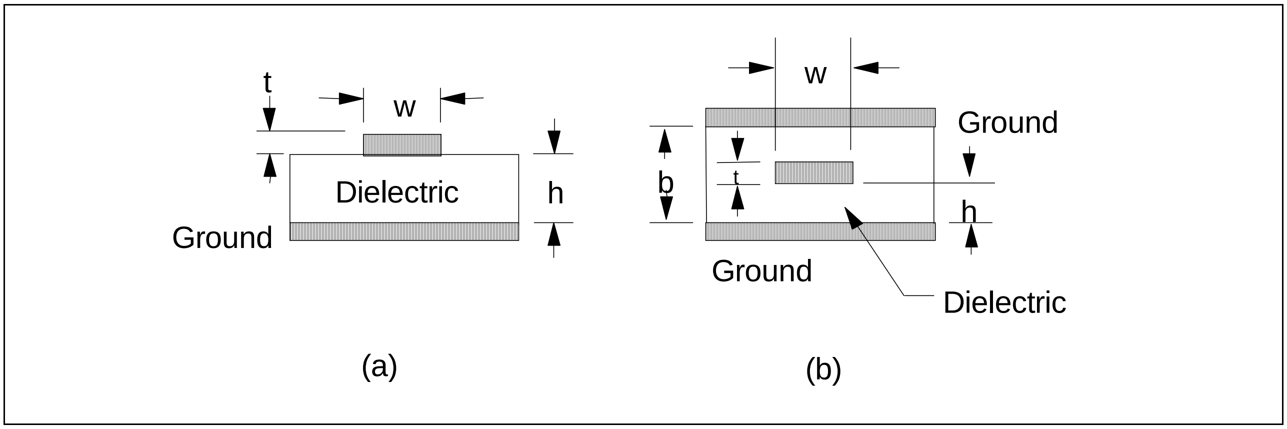

Figure C.1 - Microstrip (a) and stripline (b) geometries

C.2.1 In figure C.1 (a), a cross section of a microstrip transmission line is shown. The signal line of width *w* and thickness *t* lies on top of the surface of the dielectric layer with relative dielectric constant ε_r (typically between 4 and 5 for glass-epoxy boards) at a height of *h* above a ground or other reference plane. The characteristic impedance of a signal line with such a structure is given by the following equation. 1)

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r} + 1.41} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

C.2.2 This value is approximate, in that it assumes that the conductor is surrounded on three sides by air; if the conductor is covered by solder mask or other material (as is typical), the higher dielectric constant of that material will lower the impedance from the value calculated using the equation.

C.2.3 The stripline structure shown in figure C.1 (b) is one in which the signal line is surrounded by the dielectric material, with ground or reference planes on two sides. The characteristic impedance for the stripline structure is given by the following equation. 2)

$$Z_0 = \frac{60}{\varepsilon_r} \ln\left(\frac{4b}{0.67\pi\omega\left(0.8 + \frac{t}{w}\right)}\right)$$

C.2.4 A similar structure also exists where the conductor in question is inside the surface of the printed circuit board but is only adjacent to a ground or reference plane in one direction. This is referred to variously as “buried” microstrip or “covered” microstrip, and is shown in figure C.2.

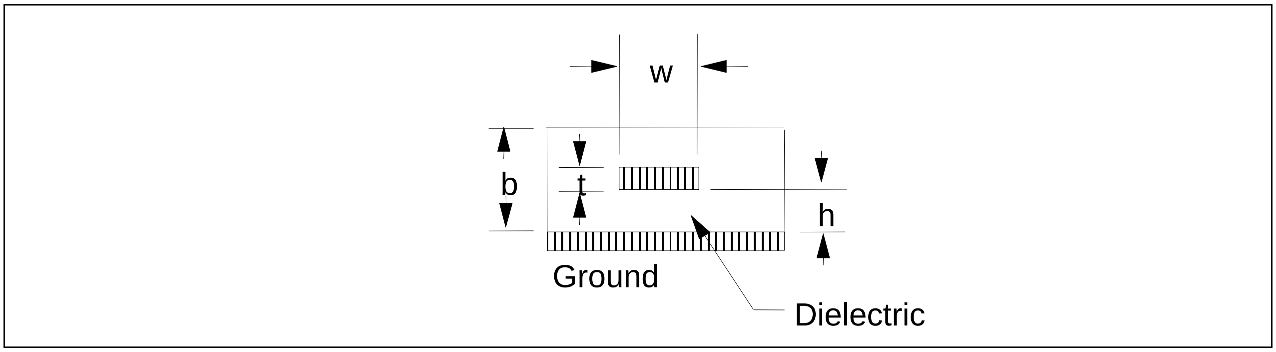

Figure C.2 - Buried microstrip geometry

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1) Blood, William R., Jr.: MECL System Design Handbook (Phoenix, AZ: Motorola Semiconductor Products, Inc., 1988), p. 45.
2) Op. cit., p. 48.

C.2.4.1 The characteristic impedance for this configuration is given by the following equation. 3)

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{5.98h}{0.8w+t}\right)$$

C.2.5 The equations above have all dealt with single-ended (unbalanced) signal lines. In the case of differential (balanced) signals, the impedance is more difficult to compute than the conventional single-ended impedance; the use of field solver software is often necessary to solve this type of problem. The use of vias is to be discouraged where possible, as the capacitance of vias causes impedance mismatches and consequent reflections in the signal path. In the event that surface ground planes are used to construct stripline structures, the surface and buried ground planes should be connected together by vias spaced no more than λ/8 apart, to prevent resonances and other undesired effects on the printed circuit board. Typically, the value for λ is the highest frequency at which measurements are to be taken.

C.2.6 Attenuation of high frequency signals (or higher order harmonics of non-sinusoidal signals) due to the so-called skin effect is a well-known phenomenon. Skin effect becomes significant when the skin depth δ is less than approximately one third of the conductor thickness. 4) For example, the skin depth in meters for copper at a given frequency of interest is given by $\delta = 0.0660/\sqrt{f}$ 5), or approximately 2.1 μm at 1 GHz. Assuming 0.035 mm or 35 micrometers (0.0014 inch (1.4 mils)) thick, (commonly referred to as “one ounce” copper) conductors typically used for printed circuit board trace, this would indicate that skin effect would be significant at frequencies above approximately 30 MHz.

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3) Buchanan, James E.: BiCMOS/CMOS Systems Design (New York: McGraw-Hill, 1991), op. cit., p. 109.

4) Deutsch, A.: “Electrical Characteristics of Interconnections for High-Performance Systems,” Proceedings of the IEEE, vol. 86, no. 2, February, 1998.

5) Ramo, S., Whinnery, J. R., and Van Duzer, T.: Fields and Waves in Communications Electronics (New York: Wiley, 1969), p.289.

C.2.7 Another effect that should be considered is resonance. Resonance can cause unexpected results, and even oscillations in the device/fixture. This effect is not just manifested at the frequencies of the exciting signals, but also at harmonics of those frequencies present in the exciting signal; the spectral content of square or nearly square pulses can extend far beyond the expected maximum frequency. The maximum frequency of significant spectral content can be estimated *as* $f_{max} = 1/\pi t_r$, where t_r is the rise or fall time of the exciting signal. 6)

> NOTE — This is independent of the period of the signal. So, for a 100 MHz signal with a rise time of 1 ns, significant spectral energy exists in that signal up to approximately 300 MHz. The "critical length" at which a printed circuit board trace may cause problems due to resonance effects is given by the following equation. 7)

$$l_{crit} = \frac{t_r}{2t_{pd}}$$

where:

t_r is the rise time of the signal and t_{pd} is the propagation delay in the medium (in the typical case, glass-epoxy). This propagation delay is typically 80-100 ps/cm (200-250 ps/in.) on inside planes of printed circuit boards, and 55 ps/cm (170 ps/in.) on outside planes, resulting in a critical length of approximately 6 cm (2 in.) for a signal rise time of 1 ns.

C.2.8 The length to be used for calculating resonance is the wavelength λ of the frequency of interest in the medium, which is given by the following equation.

$$\lambda = \frac{v}{f}$$

where:

v is the velocity in the medium and f is the frequency of interest. The velocity in the medium is the reciprocal of the propagation delay, or approximately (1-2)x10^{10} cm/s (4-8x10^{9} in./s), resulting in a wavelength of approximately 50 cm (20 in.) at 300 MHz.

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6) Ott, Henry W.: Noise Reduction Techniques in Electronic Systems (NewYork: Wiley, 1976), p. 111.

7) Buchanan, op. cit., p. 125.

C.2.9 Crosstalk should be considered in the printed circuit board design, most obviously when designing a fixture for measurement of crosstalk, but also for others. The amount of crosstalk introduced is dependent on conductor geometry (width, spacing, and height above ground) as well as the coupling length, so it is difficult to give specific guidance. The reader is referred to 8) for a discussion of the subject. A rule of thumb is that conductor spacing should be three times the conductor width to minimize crosstalk.

C.2.10 Attention shall also be paid to the trace delay, especially when designing fixtures for measurement of propagation delay. Where trace length shall be added to equalize delay between paths on the fixture, sharp corners and serpentine wiring are not to be used. Sharp corners and serpentine wiring introduce impedance mismatches into the paths, and serpentine wiring changes the propagation delay per unit length due to the coupling between adjacent legs of the pattern. This will cause actual delays that are difficult to quantify.

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8) Ibid., pp. 114-122.

Other excellent references on these subjects include:

Johnson, H. and Graham, M.: High-Speed Digital Design, a Handbook of Black Magic (Upper Saddle River, NJ: Prentice-Hall, 1993)

Matick, R. E.: Transmission Lines for Digital and Communications Networks (Piscataway, NJ: IEEE Press, 1995)

D. Mutual inductance coupling coefficient test procedure (informative)

In addition to the loop inductance measurement, described in the above procedure, and the self and mutual inductance parameters that were referenced, another inductance related parameter is the mutual inductance coupling coefficient. The mutual inductance coupling coefficient is essentially the coupling (or crosstalk) between two current loops due to the magnetic fields created by the currents in both loops. The test method for mutual inductance coupling coefficient is included here.

D.1 Set the vector network analyzer to measure S_{12} for mutual inductance.

D.2 Calibrate the equipment and fixture according to the manufacturer's specifications using the calibration standard. The calibration plane should be directly at the probe tip interface to the fixture.

> NOTE —— Due to the low inductance value being measured, it is recommended that microprobes be used.

D.3 Unless otherwise specified in the referencing document it is recommended that the following equipment settings be used:

- linear magnitude format,
- set network analyzer to display inductance values,
- minimum of 401 measurement points,
- frequency span – conduct both wideband and narrowband sweeps,
- no smoothing,
- averaging set to 16 or higher.

NOTE — "Wideband" sweep is typically the full range of the network analyzer and "narrowband" sweep is over a limited range (for example 100 MHz wide).

D.4 Fixture measurement

Position the microprobe tips to touch the interface pads of the fixture inductance calibration trace. Measure and record the inductance of the fixture from the chart at the frequency(s) of interest.

NOTE — If specified in the referencing document, an inductance vs. frequency graph may be generated through the use of data acquisition software and spreadsheet software.

D.5 Specimen measurement

D.5.1 Connect the microprobe attached to port 1 of the vector network analyzer to the first fixture interface pad. Connect the microprobe attached to port 2 of the vector network analyzer to the second fixture interface pad, with the specimen installed, as shown in figure D.1. This arrangement will allow measurement of the loop inductance between the two pads to which the probes are connected. (The microprobe plus specimen installation should be such that it terminates the far end of the driven lines in an electrical short circuit to the return conductor(s). The short circuit may be achieved by using a copper block to minimize any additional inductance.)

D.5.2 Place the specimen a minimum of 5 cm from any object that may introduce error into the measurement.

D.5.3 Measure and record the S_{12} values over the specified test frequency range or discrete frequencies.

> NOTE — If specified in the referencing document, an inductance vs. frequency graph may be generated through the use of data acquisition software and spreadsheet software.

D.5.4 Calculate the mutual inductance coupling coefficient K_m using the following equation:

$$K_m = \frac{\{3.98 \mid S_{12} \mid\}}{\{f * L\}}$$

where:

f = test measurement frequency
L = measured loop inductance

> NOTE — The preceding equation was derived from circuit analysis by looking at the time domain differential equations for a simplified, first order effect two terminal electrical short circuit.

D.6 If requested, repeat D.5 through D.5.4 on multiple lines throughout the specimen.

D.7 When additional measurements with different test frequencies or ranges are required perform the calibration step defined in D.4, then repeat D.5 through D.6 as necessary.

Figure D.1 – Example of mutual inductance coupling coefficient measurement setup

E. Loop, Mutual, and Self Inductance (Informative)

E.1 Annex provides a general overview of the differences between loop inductance, mutual inductance, and self inductance. Although this particular test method pertains specifically to loop inductance (in the range of 1 nH to 10 nH), it is important to understand the differences between all three inductance parameters as they are tightly related, both physically and mathematically, but describe different properties of conductors.

E.2 As an alternating current flows through a conductor (i.e., a terminal in an interconnect), the current causes a magnetic field or magnetic flux around the conductor. This magnetic property of a conductor, can be described by the electrical parameter inductance. The term inductance is used to describe the property of a conductor or circuit element that opposes the change in current flow. Inductance causes current changes to lag behind voltage changes, and is measured in units of Henries (Webers/Amp). The following brief descriptions are provided to distinguish the difference between several different 'types' of inductances that are used to describe the electrical characteristics of conductors and interconnects.

E.3 Interconnects (and other circuit constructions) are typically characterized by three different types of inductances; loop inductance, self inductance, and mutual inductance. Although other 'types' of inductances can be used, i.e., internal inductance (used for material characterization in electromagnetic field theory), and partial inductance (used for theoretical calculations and analytical modeling techniques), only the loop inductance, self inductance and mutual inductance parameters will be discussed here. Also, although all three of these inductances are related both physically and mathematically to each other (as will be shown), they each have significantly different meanings, and their values describe significantly different characteristics of the interconnect (or circuit element). When specifying or reporting an inductance value for an interconnect, one should be careful to clearly define which 'type' of inductance is being referenced.

E.4 These specific inductances, loop, self, and mutual, can be better described if we consider two conductors, i.e., a pair of terminals within an interconnect. One of the conductors is the signal terminal, and the other conductor is the return path terminal for the noted signal. Current is fed into the signal terminal, and creates a magnetic field around that conductor. Also, this current is returned through the return terminal, and creates another magnetic field around the return path conductor. It is this conductor arrangement and current path convention, as shown in figure E.1, which will be used to describe the inductance parameters noted.

E.5 The loop inductance parameter is most typically used to characterize interconnect performance, and can provide a representation of the intended application performance. This is due to the fact that the signal and return path currents, mutual inductances, and terminal self inductances are taken into consideration for the measurement. Although, other types of inductance measurements and parameters are important and can be very useful, it is typically the loop inductance that can most readily be directly measured.

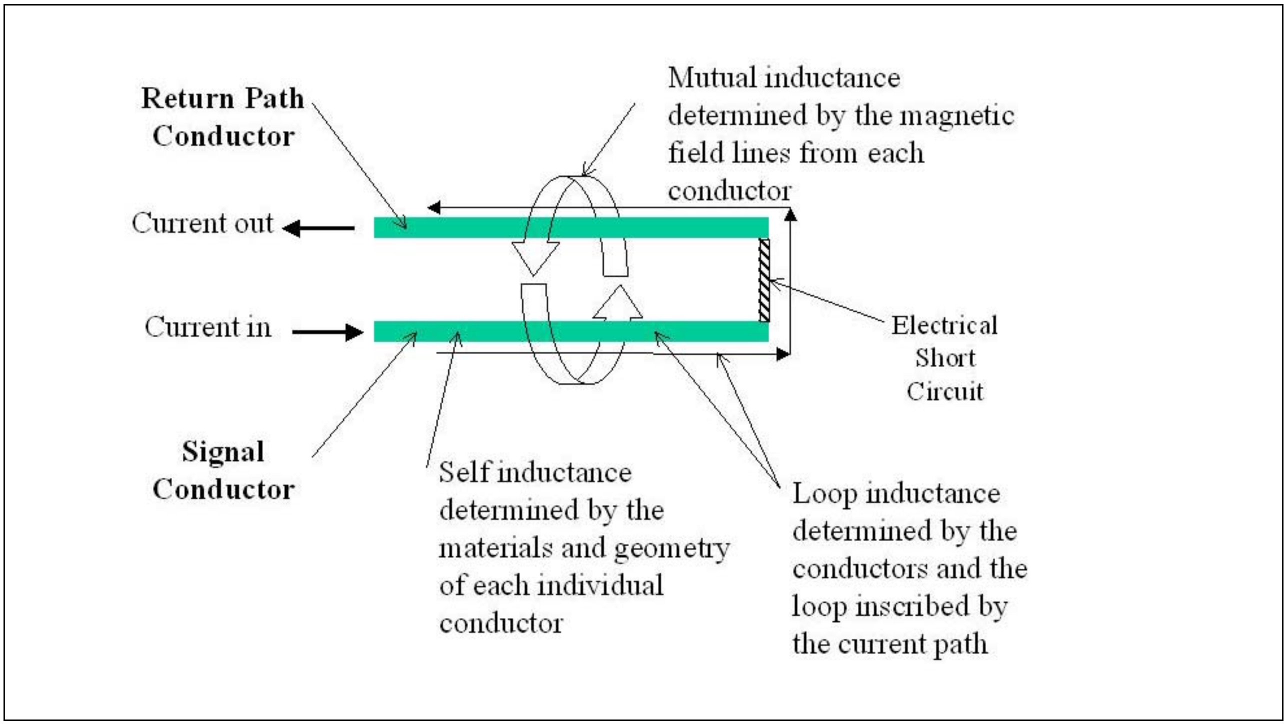

Figure E.1 - Conductor arrangement and current path convention for description of inductance

E.6 As noted above, all three of these inductances are related mathematically as shown in the following equation:

$$L_{Loop} = L_1 + L_2 \pm \left(2 * L_m\right)$$

where: L_1 = self inductance of the driven conductor
L_2 = self inductance of the return path conductor(s)
L_m = mutual inductance between the drive and return path conductors.

E.7 The ± symbol in the above equation is used to take into account the relative direction in which the currents in the terminals are traveling. The minus sign is used for the case when the currents are traveling in opposite directions. The plus sign (which is not used specifically in this test method) is used for the case when the currents are traveling in the same direction. This equation demonstrates that for currents traveling in opposite directions, the overall loop inductance is actually decreased as the mutual inductance is increased. However, for currents traveling in the same direction, as the mutual inductance is increased, the overall loop inductance is also increased. This effect should be noted, and reviewed while tests are conducted as the current direction and return paths will have significant effects on the overall loop inductance measured value.

E.8 In contrast to loop inductance, the self inductance parameter is used to describe the inductance of a single conductor, ideally in free space. Self inductance of a single conductor is based on the material properties and geometry of the conductor and does not take into consideration materials around the conductor or other conductors or currents. Self inductance is also a very important circuit parameter, and can be used for simulations and calculations effectively when the value is known. However, self inductance in ranges below approximately 20 nH (a range covering many electrical connectors and sockets) is very difficult to measure due to practical limitations of test equipment, calibration structures, and test fixtures. Some of the main issues with obtaining an empirical, accurate measurement of self inductance in this range include:

- obtaining an ideal short over a distance in which the inductance of the short can be considered zero,
- obtaining test equipment in which the resolution would allow measurements to be made accurately at 1-20 nH,
- providing a test fixture in which fixture test currents are not allowed to interact with the conductor or terminal being tested.

E.9 However, with the use of both modeling techniques and measurement data, self inductance can be calculated from the above equation utilizing the measurement data and the calculated data.

E.10 Mutual inductance is also an important circuit parameter, and effects the loop inductance and thus the performance of an interconnect. Mutual inductance is related to the magnetic field interactions that are generated by currents flowing in two or more conductors. Mutual inductance is determined by the materials and geometries of the entire current path structure including both the conductors and the areas surrounding the conductors. Therefore, mutual inductance is very tightly related to the loop inductance and self inductance parameters described above. Again, as seen in the loop inductance equation, the self inductance of the terminals can remain the same, and by either increasing or decreasing the mutual inductance between the terminals, the loop inductance can be changed.

E.10.1 The test professional should be aware of these potential changes during the inductance measurement. Due to the fact that mutual inductance is a function of the magnetic fields, which are generated by current flowing in the conductors, care should be taken to minimize the interaction between the test fixture and the specimen. More specifically, the magnetic field interactions generated as a result of the current in the test fixtures, should be reviewed as it can have significant effects on the measurement.

E.10.2 Similar to the reasons given for making a low level self inductance measurement, the mutual inductance parameter is also very difficult to measure in such low values as are encountered in typical electrical interconnects. As an example, for typical board to board or edge card type connectors, the mutual inductance parameter may be approximately 10% - 15% of the loop inductance value. However, again similar to self inductance, mutual inductance can be calculated from the a combination of measurement data (typically the loop inductance) and calculations or modeling by using the loop inductance equation.

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