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EIA STANDARD

TP-108

Impedance, Reflection Coefficient, Return Loss, and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Cable Assemblies or Interconnection Systems

EIA-364-108

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Electronic Components, Assemblies & Materials Association

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(From Standards Proposal No. 4454-A, formulated under the cognizance of the CE-2.0 National Connector Standards Committee.)

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TEST PROCEDURE No. 108

IMPEDANCE, REFLECTION COEFFICIENT, RETURN LOSS, AND VSWR MEASURED IN THE TIME AND FREQUENCY DOMAIN TEST PROCEDURE FOR ELECTRICAL CONNECTORS, CABLE ASSEMBLIES OR INTERCONNECTION SYSTEMS

(From EIA Standards Proposal No. 4454-A, formulated under the cognizance EIA CE-2.0 Committee on National Connector Standards.)

1 Introduction

1.1 Scope

This procedure applies to interconnect assemblies, such as electrical connectors, and cable assemblies.

1.2 Object

This standard describes test methods to measure impedance, reflection coefficient, return loss, and voltage standing wave ratio (VSWR) in the time and frequency domains.

NOTE — These test methods are written for test professionals who are knowledgeable in the electronics field and are trained to use the referenced equipment. Because the measurement values are heavily influenced by the fixturing and equipment this method cannot describe all of the possible combinations. The major equipment manufacturers provide Application Notes for more in-depth technical description of how to optimize the use of their equipment. It is imperative that the referencing document include the necessary description and sketches for the test professional to understand how to setup and perform the requested measurements.

1.3 Definitions

1.3.1 Measurement system rise time

Rise time measured with the fixture in place, without the specimen, and with filtering (or normalization). Rise time is typically measured from 10% to 90% levels.

1.3.2 Specimen environment impedance

The impedance presented to the signal conductors by the fixture. This impedance is a result of transmission lines, termination resistors, attached receivers or signal sources, and fixture parasitics.

1.3.3 Reflection coefficient

The ratio of the reflected to incident voltages at any given point. The reflection coefficient is given by:

$$\text{Gamma } (\Gamma) = \frac{V_{reflected}}{V_{incident}} = \frac{Z_L - Z_O}{Z_L + Z_O} = s_{11}$$

where Z_L is the fixture or specimen impedance and Z_O is the specimen environment impedance.

NOTE — In the time domain, the reflection coefficient symbol typically used is rho (ρ), while Gamma (Γ) is used for frequency domain measurements.

1.3.4 Impedance

The total opposition that a circuit offers to the flow of alternating current or any other varying current at a particular frequency. It is a combination of the resistance (R) and reactance (X) measured in ohms (Ω). The equation for impedance as a function of s-parameters is:

$$Z = Z_0 \frac{1 + s_{11}}{1 - s_{11}} = R + jX = Z_0 \left[\frac{(1 + \text{rho})}{(1 - \text{rho})} \right]$$

1.3.5 Return loss

The ratio in decibels (dB) of the power incident upon the impedance discontinuity to the power reflected from the discontinuity. The equation for return loss calculated from the reflection coefficient is:

$$\text{Return Loss} = 20 \log_{10} |\Gamma| = 20 \log_{10} |s_{11}|$$

1.3.6 Voltage Standing Wave Ratio (VSWR)

The ratio of the maximum magnitude of the voltage on a line to the minimum magnitude at any given point. VSWR can be expressed by the following equations:

$$\text{VSWR} = \frac{|V_{max}|}{|V_{min}|} = \frac{|V_{inc} + V_{refl}|}{|V_{inc} - V_{refl}|}$$

or

$$\text{VSWR} = \frac{(1 + |\Gamma|)}{(1 - |\Gamma|)}$$

1.3.7 Scattering parameter (s-parameter), s_{11}

The reflection coefficient at the input port of the device under test, defined as the ratio of the reflected voltage to the incident voltage.

1.3.8 Termination (electronics usage)

An impedance connected to the end of a transmission line, typically to minimize reflected energy on the line.

1.3.9 Step amplitude

The voltage difference between the 0% and 100% levels, ignoring overshoot and undershoot.

2 Test resources

Care should be taken when establishing the equivalence between time and frequency domain measurements. The relationship between the two is complex and the application of bandwidth = (0.35/rise time) should not be used without further computations and understanding.

2.1 Equipment

2.1.1 Time domain

2.1.1.1 A Time Domain Reflectometer (TDR) is preferred, although an oscilloscope and pulse generator may be used. A network analyzer may be used with FFT (Fast Fourier-Transform) software.

NOTE — The test professional should be aware of limitations of any math operation performed by an instrument (e.g., FFT).

2.1.1.2 Variable rise time

A means should be provided for varying the signal rise time if required. This may be included within the test equipment itself, or possibly through additional filtering or software.

NOTE — The test professional should be aware of limitations of any math operation performed by an instrument or software; e.g., normalization or filtering.

2.1.1.3 Differential measurements

The test equipment shall have the capability to perform differential measurements directly, or provisions shall be made to calculate the impedance from multiple single-ended measurements.

2.1.2 Frequency domain

2.1.2.1 A vector network analyzer or impedance analyzer shall be used.

NOTES

1 The test professional should be aware of the frequency limitations of the fixture.
2 The test professional should be aware of any limitations of any mathematical functions performed (e.g., normalization, inverse FFT, or software filtering.)

2.1.2.2 Differential measurements

For differential measurements, a network analyzer and baluns may be used.

NOTE — The test professional should be aware of the electrical characteristics of the baluns, that become part of the test fixture and can significantly affect the measurement.

2.2 Fixture

The fixture(s) shall allow for enough measurements throughout the specimen such that variations in geometries, materials, transmission paths, etc. may be demonstrated and provide a representative sampling of specimen performance.

NOTE — The fixture geometry and materials will impact the measurements due to the fixture parasitics. Usually the product's intended use dictates the most meaningful way to fixture it.

2.2.1 Specimen environment impedance

Unless otherwise specified in the referencing document, the specimen environment impedance shall match the impedance of the test equipment. Typically this will be 50 ohms for single ended measurements and 100 ohms for differential measurements.

2.2.2 Terminations

When using termination resistors, care should be taken to minimize the parasitic reactances of the terminators over the range of test frequencies; see annex E.

2.2.3 Calibration features

See annex C for calibration and reference traces.

NOTE — The term “calibration” used in this document is not to be confused with the periodic factory equipment calibration. Calibration is used in the sense of characterizing the fixture so that when the “fixture plus specimen” measurement is taken, the characteristics of the specimen alone can be accurately determined.

2.2.3.1 Time domain

The fixture shall include features such that the near and far ends of the specimen may be determined in time; see annex B. The calibration plane should be as close to the specimen as possible. When the fixture includes a pc board with line traces connecting two connectors, it shall have a reference trace(s) that will allow the measurement system rise time to be measured. The reference trace shall have starting points and endpoints at the same location as the DUT starting point and end point. This is because the reference trace(s) length shall be the same as the pc board traces.

2.2.3.2 Frequency domain

It is necessary to include fixture features that will allow for the open, short, and load measurements to be taken. This may be accomplished by one of two methods. Firstly, provide reference traces that include the open, load and short standards. Secondly, provide an interface where these standards can be applied directly to the end of the fixture and immediately before the input plane of the device under test. When using the open/short method, the fixture shall include features such that measurements may be conducted with the far end of the driven line both open-circuited and short-circuited.

NOTE — Other calibration techniques (such as Through-Reflect-Line) may be used. The fixture shall incorporate features appropriate to that calibration method(s).

2.2.4 Single-ended

The fixture shall allow one signal line to be driven at a time. The far end of the driven line shall be terminated in the specimen environment impedance (typically 50 ohms). It is recommended that a length of transmission line be added after the sample that has a propagation delay greater than twice the measurement system rise time. Unless otherwise specified in the referencing document:

— a 1:1 signal to ground ratio shall be used,
— designated ground lines shall be commoned on both the near and far end,
— adjacent signal lines shall be terminated in the specimen environment impedance.

2.2.5 Differential

The fixture shall allow one signal pair to be driven at a time. The driven pair shall be terminated in the specimen environment impedance (typically 100 ohms). It is recommended that a length of transmission line be added after the specimen that has a propagation delay greater than twice the measurement system rise time. Unless otherwise specified in the referencing document:

— a 2:1 signal to ground ratio shall be used (one signal pair for each ground return),
— designated ground lines shall be commoned on both the near and far end,
— adjacent signal lines shall be terminated in the specimen environment impedance.

NOTE — For differential applications in the frequency domain using a 2-port network analyzer, the fixture will include the use of baluns.

3 Test specimen

3.1 Description

For this test procedure the test specimen shall be as follows:

3.1.1 Separable connectors

A mated connector pair.

3.1.2 Cable assembly

Assembled connectors and cables, and mating connectors.

4 Test procedure

4.1 Time domain

4.1.1 Calibrate the equipment and fixture according to the manufacturer's specified measurement techniques using precision impedance standards and/or cabling. The calibration plane is to be directly at the input interface of the specimen; see 2.2.3.1 for more detailed information.

4.1.2 Connect the TDR signal line(s) to the reference line(s) of the test fixture.

4.1.3 Unless otherwise specified in the referencing document, the signal rise time shall be the fastest signal of which the equipment is capable. If a slower signal rise time is also desired to approximate the application conditions, one of the rise times in table 1 may be used. Measure and record the measurement system rise time from the reference line, as shown in figure A.1.

Table 1 - Additional measurement system rise time (including fixture and filtering)

Typical application rise time in which the specimen will be used, Picoseconds	Measurement system rise time, picoseconds
100 – 500	100
>500 – 1,000	500
> 1,000	1000

4.1.4 Measure, record, and plot the requested parameters for the test fixture (impedance, reflection coefficient, and/or voltage). If the equipment does not have the capability to display the requested parameter directly see the applicable clause of 1.3 for conversion equations.

4.1.5 Connect the TDR line(s) to the driven line(s) of the fixture with the specimen installed.

4.1.6 Place the specimen a minimum of 5 cm from any objects that may introduce error into the measurement.

4.1.7 Determine the near end and far end of the specimen. Annex B describes a method for determining the near and far end of the specimen.

4.1.8 Display and record the requested electrical parameter on the test equipment. If the equipment does not have the capability to display the requested parameter directly see the applicable clause of 1.3 for conversion equations. Refer to figure A.2 for example of a TDR plot, and annex D for examples of interpreting TDR impedance graphs.

4.1.8.1 Single ended measurement

Set the test equipment to display the driven signal line waveform.

4.1.8.2 Differential measurement

Set the test equipment to display a waveform representing the difference between the two driven signal line waveforms, (typically, “Trace 1 minus Trace 2”).

NOTE — If not available within the TDR equipment, this mathematical function may be accomplished by collecting the raw voltage data with an acquisition system and manipulating the data with appropriate software.

4.1.9 When required, vary the measurement system rise time and repeat 4.1.2 through 4.1.8. Record the measurement system rise times with the corresponding data.

NOTE — When varying measurement system rise times, the test professional should be aware of limitations of any math operation performed by an instrument, (e.g. normalization or software filtering).

4.1.10 If requested, repeat 4.1.5 through 4.1.9 for multiple lines throughout the specimen.

4.2 Frequency domain

4.2.1 General

4.2.1.1 Calibrate the equipment and fixture according to the manufacturer's specifications using precision impedance standards and/or cabling. The calibration plane is to be directly at the input interface of the specimen, see 2.2.3.2 for more detailed information.

NOTE — The test professional is reminded that the calibration shall be performed in the mode to be used for the measurements; e. g., s_{11}.

4.2.1.2 Fixture measurement

Set the analyzer for a single port (or comparable) measurement. Select the display mode for the desired parameter (impedance, reflection coefficient, return loss, VSWR) as specified in the referencing document. If using a network analyzer, measure and record s_{11}. Refer to figure A.3 for an example of a network analyzer plot. It is recommended that the following equipment settings be used:

— cartesian plots with a logarithmic frequency scale and linear Y-axis,
— minimum of 201 measurement points,
— maximum smoothing of 1%.

If the equipment does not have the capability to display the requested parameter directly see the applicable clause of 1.3 for conversion equations.

4.2.2 Specimen measurement - Direct method

4.2.2.1 Connect the analyzer line(s) to the driven line(s) of the fixture with the specimen installed. Terminate the far end of the test specimen in the specimen environment impedance.

4.2.2.2 Place the specimen a minimum of 5 cm from any object that may introduce error into the measurement.

4.2.2.3 Measure and record the requested parameter values over the specified test frequency range or discrete frequencies. If the equipment does not have the capability to display the requested parameter directly, see the applicable clause of 1.3 for conversion equations.

4.2.2.4 If requested, repeat 4.2.2.1 through 4.2.2.3 on multiple lines throughout the specimen.

4.2.2.5 When additional measurements with different test frequencies or ranges are required perform the calibration step defined in 4.2.1.1, then repeat 4.2.2.1 through 4.2.2.4 as necessary.

4.2.3 Specimen measurement - Open/short method

4.2.3.1 Connect the analyzer line(s) to the driven line(s) of the fixture with the specimen installed.

4.2.3.2 Place the specimen a minimum of 5 cm from any object that may introduce error into the measurement.

4.2.3.3 Place an open circuit at the far end of the specimen. Measure and record the open-circuit impedance, Z_{OC}.

4.2.3.4 Place a short circuit at the far end of the specimen. Measure and record the short-circuit impedance, Z_{SC}.

4.2.3.5 Calculate the impedance using the following equation:

$$Z = \sqrt{Z_{OC} \bullet Z_{SC}}$$

4.2.3.6 Using this calculated impedance value, it is possible to calculate other electrical parameters, such as reflection coefficient, VSWR, and return loss using the equations found in 1.3.

4.2.3.7 If requested, repeat 4.2.3.1 through 4.2.3.6 on multiple lines throughout the specimen.

4.2.3.8 When additional measurements with different test frequencies or ranges are required perform the calibration step defined in 4.2.1.1, then repeat 4.2.3.1 through 4.2.3.7 as necessary.

5 Details to be specified

The following details shall be specified in the referencing document:

5.1 Electrical parameter(s) to be measured such as impedance, reflection coefficient, VSWR, and/or return loss

5.2 Measurement system rise time(s), (if other than the fastest of which the equipment is capable) or test frequencies

5.3 Any special requirements with respect to fixture and termination construction and electrical properties

5.4 Single-ended or differential measurements

5.5 Signal/ground pattern, including the number and location of signal and grounds. It is recommended that enough locations within the specimen be measured to take into account the varying impedances within the specimen.

5.6 Specimen environment impedance if other than 50 ohms for single ended and 100 ohms for differential.

5.7 Any desired plots; e.g., TDR traces, parameter vs. frequency graphs, or Smith charts.

5.8 Minimum, maximum, or average values of the time domain parameter(s) measured or calculated for the specimen.

NOTE — When average values are requested, the minimum and maximum values shall also be reported.

5.9 Minimum, maximum, or average values of the frequency domain parameter(s) measured or calculated for the specimen over a desired frequency range or at specific frequencies.

NOTE — When average values are requested, the minimum and maximum values shall also be reported.

6 Test documentation

Documentation shall contain the details specified in clause 5, with any exceptions, and the following:

6.1 Title of test

6.2 Test equipment used, and date of last and next calibration

6.3 Method used, time domain or frequency domain. If frequency domain, if direct or open/short method was used.

6.4 Values and observations

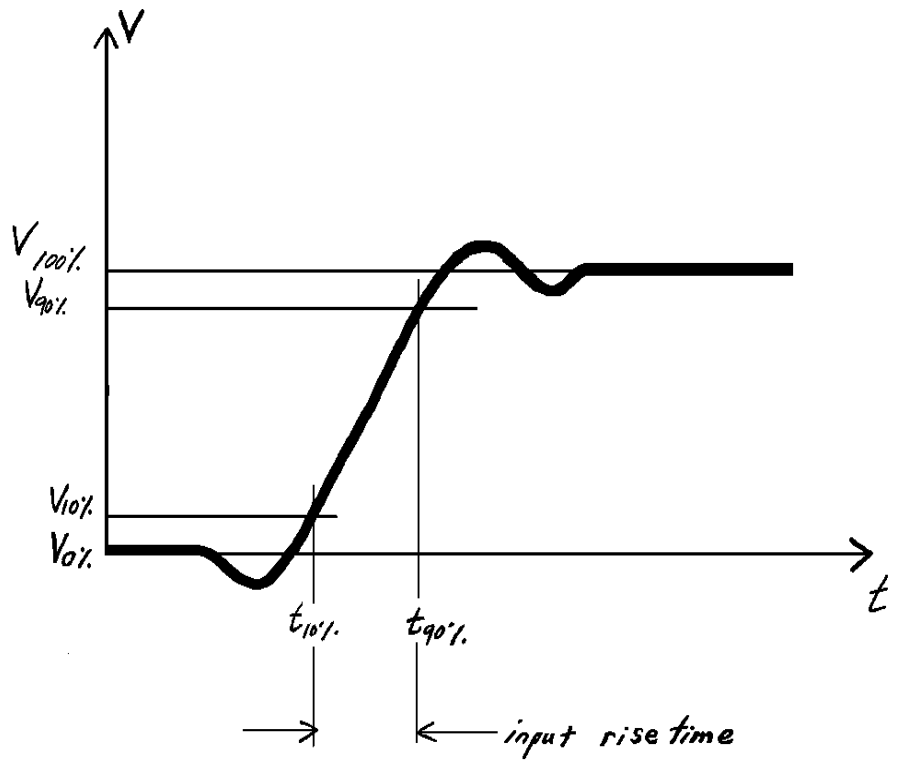
6.5 Representative graphs, if available

6.6 Name of operator and date of test

Annex A

A Measurement system rise time (normative)

When determining the measurement system rise time, it is recommended that the time scale on the TDR or oscilloscope be set to a large time per division setting. This is to ensure that the effects of any ringing or other short-term disturbances do not distort the measured 0% and 100% levels.



NOTE — Ignore overshoot and undershoot when calculating 0% and 100% levels.

Figure A.1 – Example of rise time measurement points

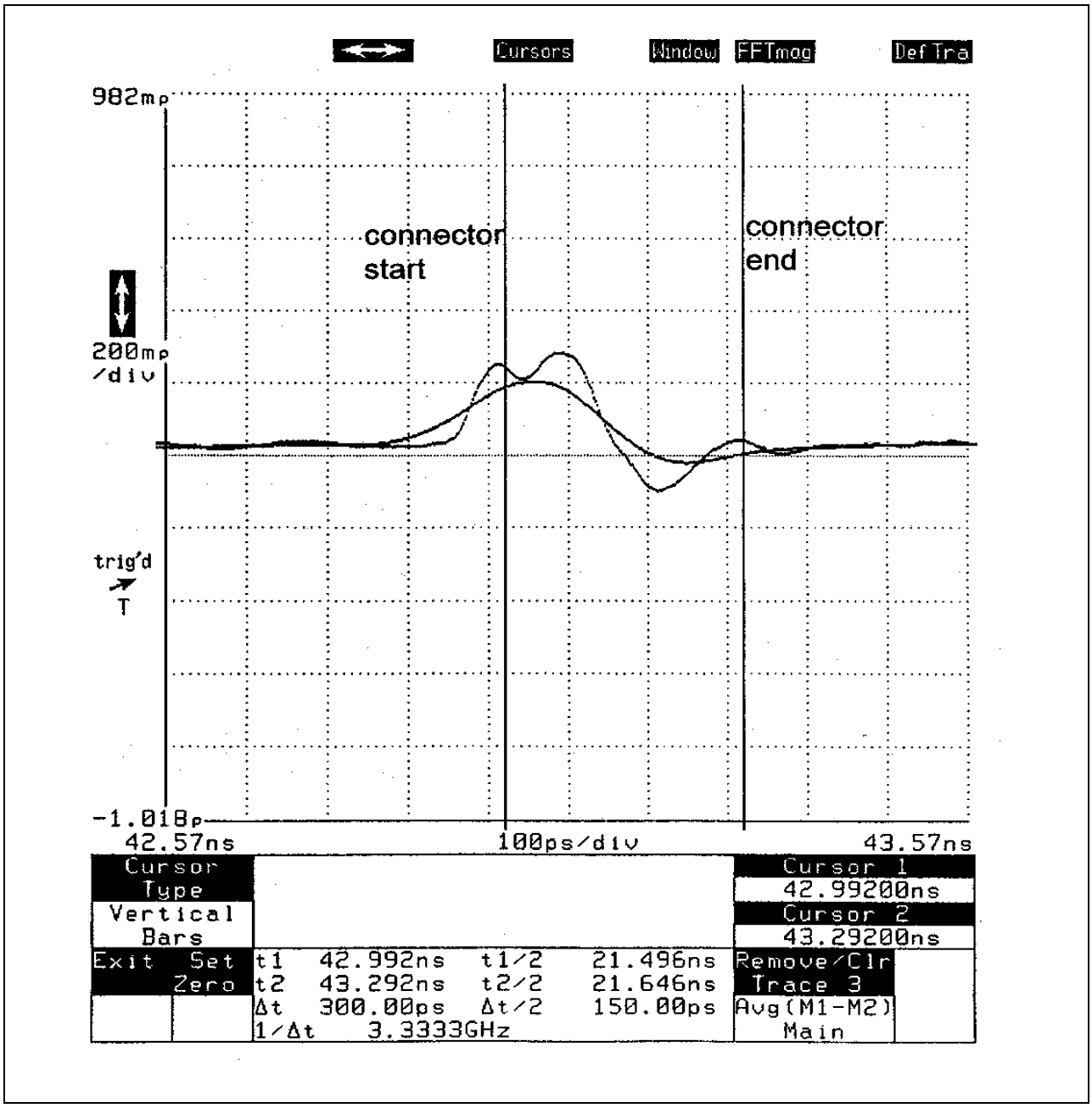


Figure A.2 – Example of TDR output; 2 curves (different rise times) and start and stop specimen points

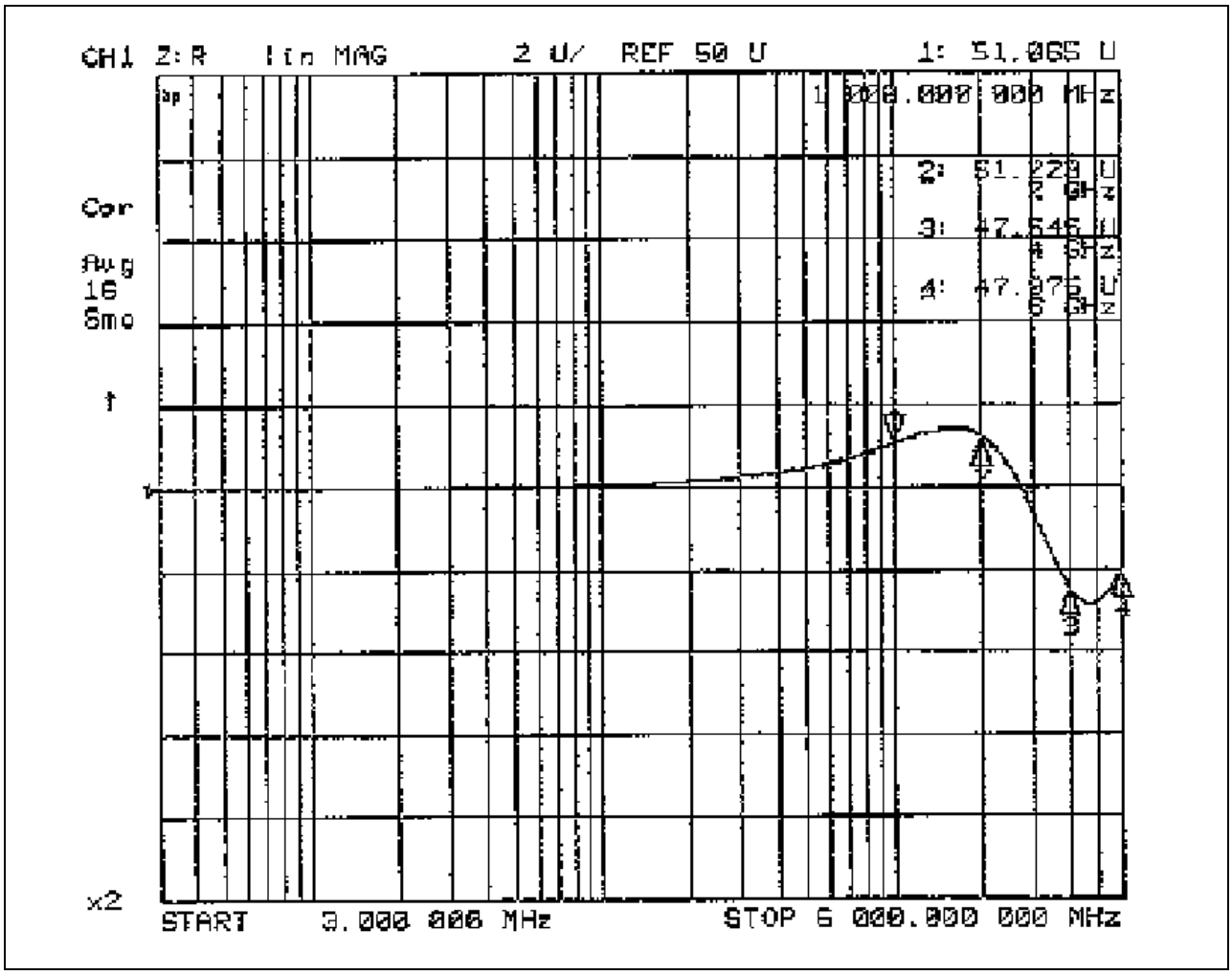


Figure A.3 – Example of analyzer output, impedance vs. log frequency plot

Annex B

B Determination of the near end and far end of the specimen (informative)

B.1 When making certain measurements it is important to be able to determine the near end (‘start’) and far end (‘stop’) of the specimen in time within the test fixture. The near end (‘start’) and far end (‘stop’) of the specimen may be determined by measuring the propagation delay of the near end of the fixture alone, the propagation delay of the far end of the fixture alone, and the propagation delay of the fixture with the specimen installed. This method is useful when a printed circuit board fixture is used.

B.2 Connect the TDR equipment to the near end reference trace as described in C.2.1.1. Observe the time on the scope at which the TDR impedance trace sharply drops. Record this time as the location in time of the near end of the specimen.

B.3 Connect the TDR equipment to the fixture with specimen installed and measure the propagation delay.

B.4 Connect the TDR equipment to the far end reference trace as described in C.2.1.1. Observe the time on the scope at which the TDR impedance trace sharply drops. The location in time of the far end of the specimen is the propagation delay of the fixture with the specimen installed minus this value.

NOTE — In “TDR mode” the propagation delay displayed is twice the actual value. In “TDT mode” the propagation delay displayed is equal to the actual value.

Annex C

C Calibration standards and test board reference traces (informative)

C.1 Calibration standards

C.1.1 For the equipment calibration, a traceable calibration impedance standard should be used for a reference baseline. Specific equipment calibration should be performed according to the manufacturer's instructions. However, care should be taken as to what standards or other fixtures are used for the calibration procedure.

NOTE — The term "calibration" used in this document is not to be confused with the periodic factory equipment calibration. Calibration is used in the sense of characterizing the fixture so that when the "fixture plus specimen" measurement is taken, the characteristics of the specimen alone can be accurately determined.

C.1.2 When possible the fixture should be designed to allow the attachment of the calibration standard as close to the specimen as possible. Reflections from fixture imperfections increase measurement error.

C.1.3 Printed circuit test boards should not be used as calibration standards. Because of different printed circuit board technologies, fabrication control, and material variations, it becomes difficult to insure that different board designs or fabrication techniques will have the same calibration reference for the impedance measurements. The impedance value of "controlled impedance traces" on a printed circuit board is typically ± 10% or ± 5% of the target value. In measurements and applications, this may be an acceptable tolerance to hold, however, for calibration purposes, this should not be used as a baseline.

C.2 Test board reference traces

The use of the traceable standard termination at the end of the test cable will allow the test fixture printed circuit board effects to be measured more accurately. The test professional will be able to accurately measure the impedance or transmission characteristic of the printed circuit board fixture, and not allow the test equipment to try to compensate for any fixture discontinuities.

Figures C.1 and C.2 show single ended test boards for a board-to-board connector using SOLT calibration trace structures. Calibration using other methods, for example TRL, will require different structures.

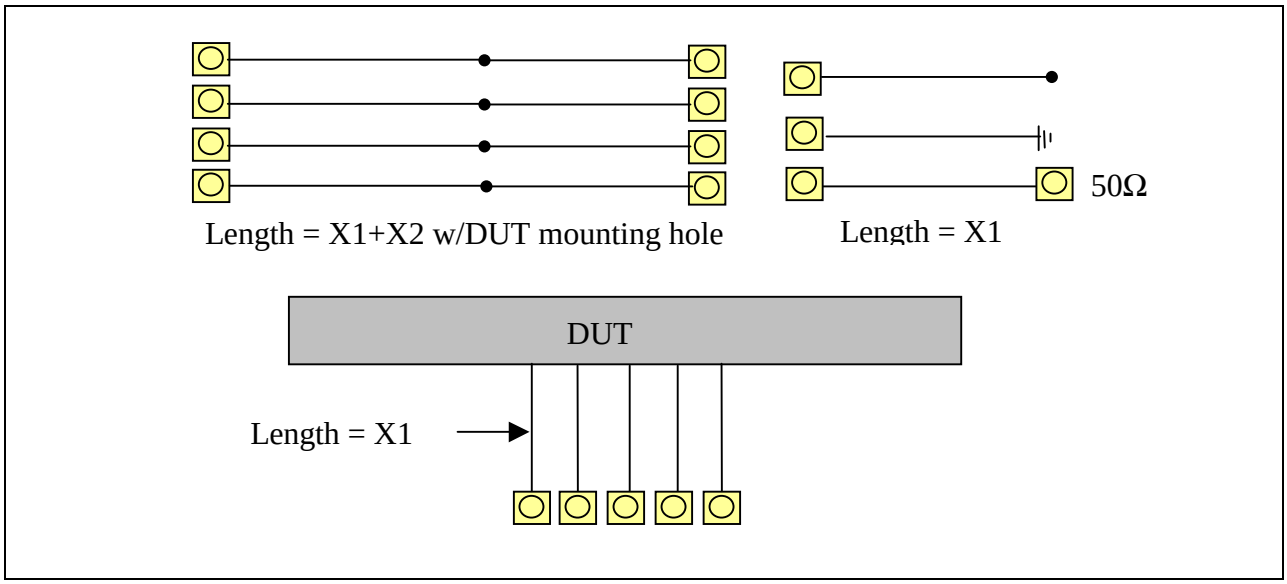
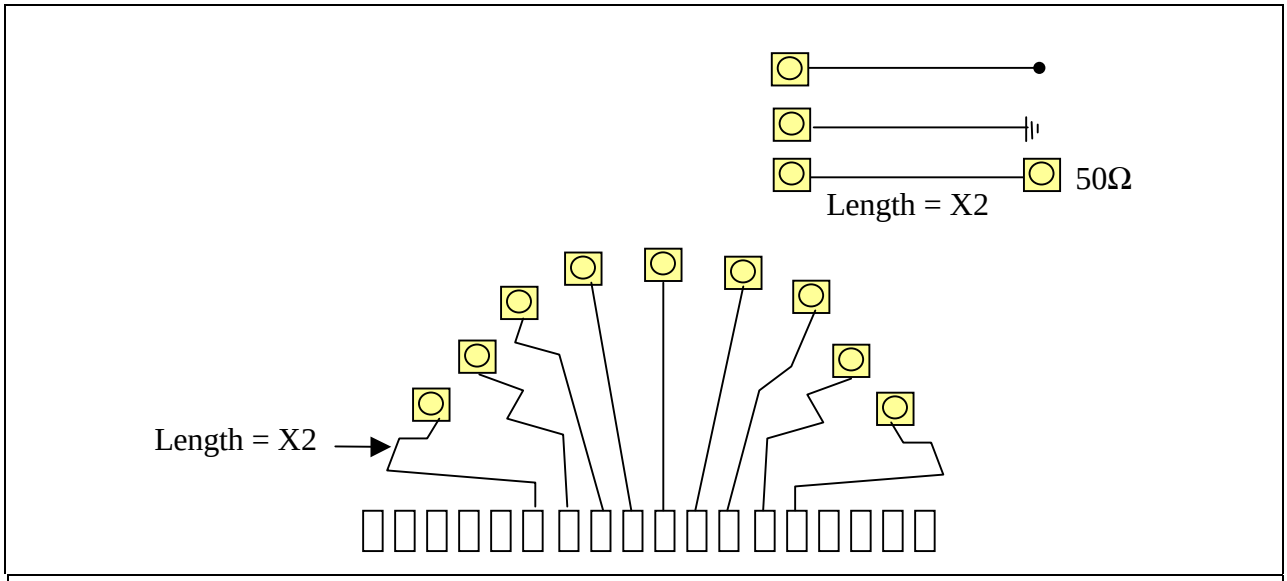


Figure C.1 –Typical mother board test fixture



NOTE — Conductor traces are not made with sharp corners. They are only shown this way to illustrate designing equivalent length traces.

Figure C.2 – Typical daughter board test fixture

C.2.1 Time domain

Test boards shall include reference traces for measuring the measurement system rise time and amplitude of the TDR system step signal, including the effects of the test fixture, as well as the TDR signal source and sampling head response times. Note that using this measured step amplitude for normalizing the connector reflections will correct for some of the effects of impedance level mismatch between the TDR system/cable, and the test board at the near end.

Recommended test fixture configurations:

C.2.1.1 A reference trace ending in a via which is shorted to the appropriate reference plane layer. The length of this reference trace should be the same as that of the trace connected to the near end of the device under test.

C.2.1.1.1 The effective step signal rise time and amplitude are equal to the TDR measured values of the amplitude and fall time of the negative step reflection at the short circuit termination at the far end of this reference trace. When the impedance of the test board does not precisely match the impedance of the TDR head and test cable, the falling transition from the zero reflection level to the “short circuit” or “-1 rho” level includes additional positive or negative step portions. The recommended waveform portion for measuring the effective test system amplitude and fall time is indicated in figure C.3.

C.2.1.2 A reference trace ending in a via which is open with respect to the appropriate reference plane layer. The length of this reference trace should be the same as that of the trace connected to the near end of the device under test.

C.2.1.3 A reference trace ending in a via to the specimen environment impedance. The length of this reference trace should be the same as that of the trace connected to the near end of the device under test.

C.2.1.4 A straight through transmission trace whose length is equal to the total fixture trace length for a single path, (length of the near end and far end traces). The test fixture shall provide an identical coaxial cable or probe connection at both ends.

C.2.1.4.1 In this case the TDR system’s effective rise time and amplitude when used with the fixture board are determined from a TDT measurement of this reference trace (measurement system rise time). When the impedance of the test boards does not precisely match impedance of the TDR, a second delayed step will appear on the transmitted step waveform. The recommended portion of the waveform for measuring the effective test system amplitude and rise time is indicated in figure A.1.

NOTE — The test board should include a reference structure (including footprint pads, grounds, traces, vias) with the same configuration as the device under test would have in a typical end use application.

C.2.2 Frequency domain

Test boards shall include reference traces for measuring the frequency domain characteristics of the fixture in order to correct for fixture effects (e.g., discontinuities in impedance). Various calibration techniques such as SOLT (Short-Open-Load-Through) and TRL (Through-Reflect-Line) may be used. The fixture shall incorporate features appropriate to that calibration method(s). Recommended test fixture configurations for the commonly used SOLT method include:

C.2.2.1 A reference trace ending in a via which is shorted to the appropriate reference plane layer. The length of this reference trace should be the same as that of the trace connected to the near end of the device under test.

C.2.2.2 A reference trace ending in a via which is open with respect to the appropriate reference plane layer. The length of this reference trace should be the same as that of the trace connected to the near end of the device under test.

C.2.2.3 A reference trace ending in a via to the specimen environment impedance. The length of this reference trace should be the same as that of the trace connected to the near end of the device under test.

C.2.2.4 A straight through transmission trace whose length is equal to the total fixture trace length for a single path, (length of the near end and far end traces). The test fixture shall provide an identical coaxial cable or probe connection at both ends.

NOTE — The test board should include a reference structure (including footprint pads, grounds, traces, vias) with the same configuration as the device under test would have in a typical end use application.

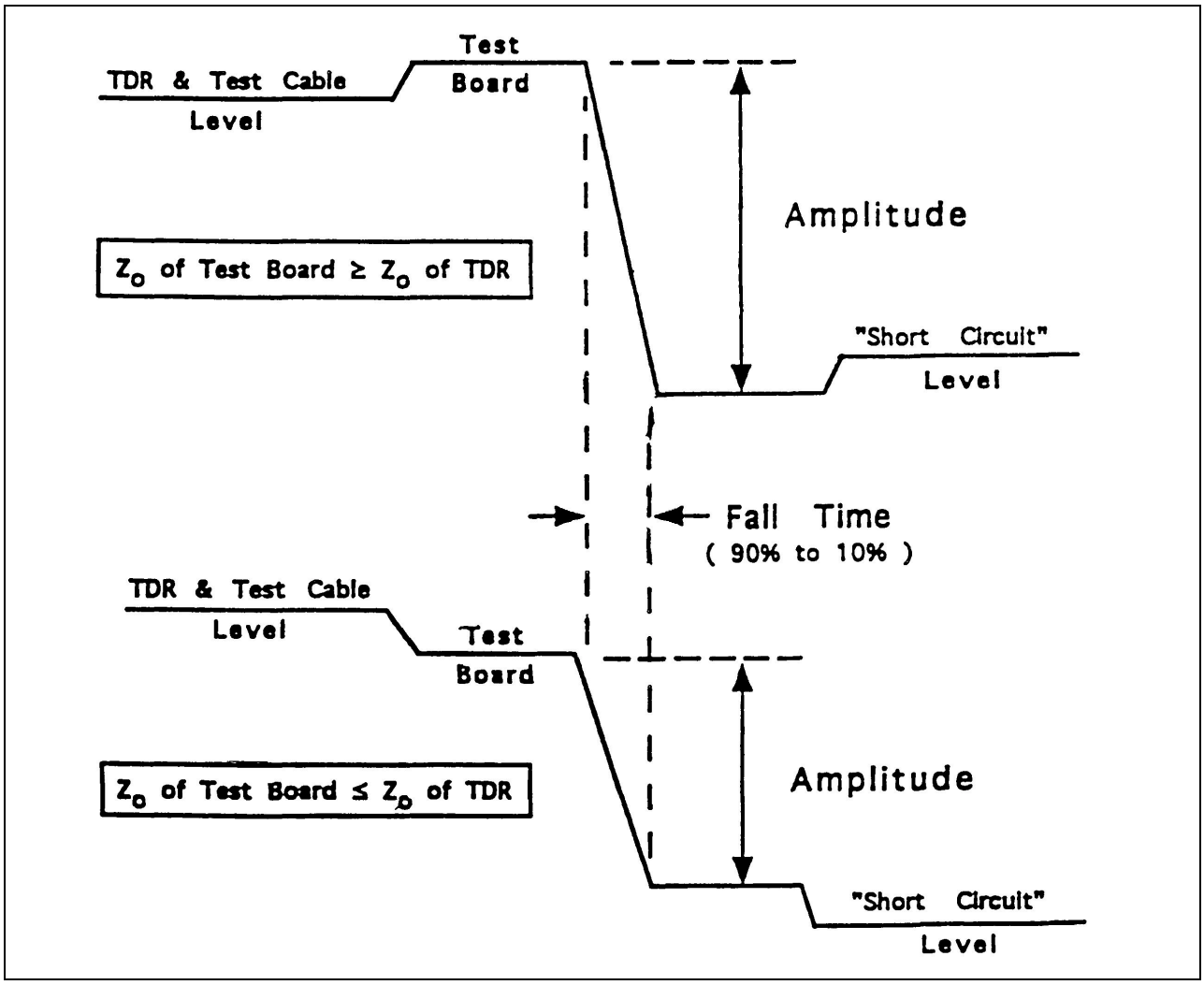


Figure C.3 – Example of near end reference trace

Annex D

D Interpreting TDR impedance graphs (informative)

Figures D.1 and D.2 are examples of various TDR impedance graphs and a brief explanation of each. It is beyond the scope of this document to describe all the fine points of interpreting TDR plots. Significant measurement errors may be introduced by lossy test fixtures, etching problems with board traces, dielectric variations in the test board and others.

D.1 Example of TDR trace

Figure D.1 demonstrates an example of a TDR trace (impedance profile) including an SMA connector, PCB fixture motherboard, interconnect specimen, PCB fixture daughter board, and then an open termination. From this TDR graph the test professional can determine, for example, the start and stop of the connector (remembering the TDR time measurements are the round trip, go and return), minimum and maximum impedance values of the device under test, and average impedance of the specimen. It should be noted that each TDR trace is specific to the measurement system rise time at which it was measured, and this information should always be reported with the measured impedance values.

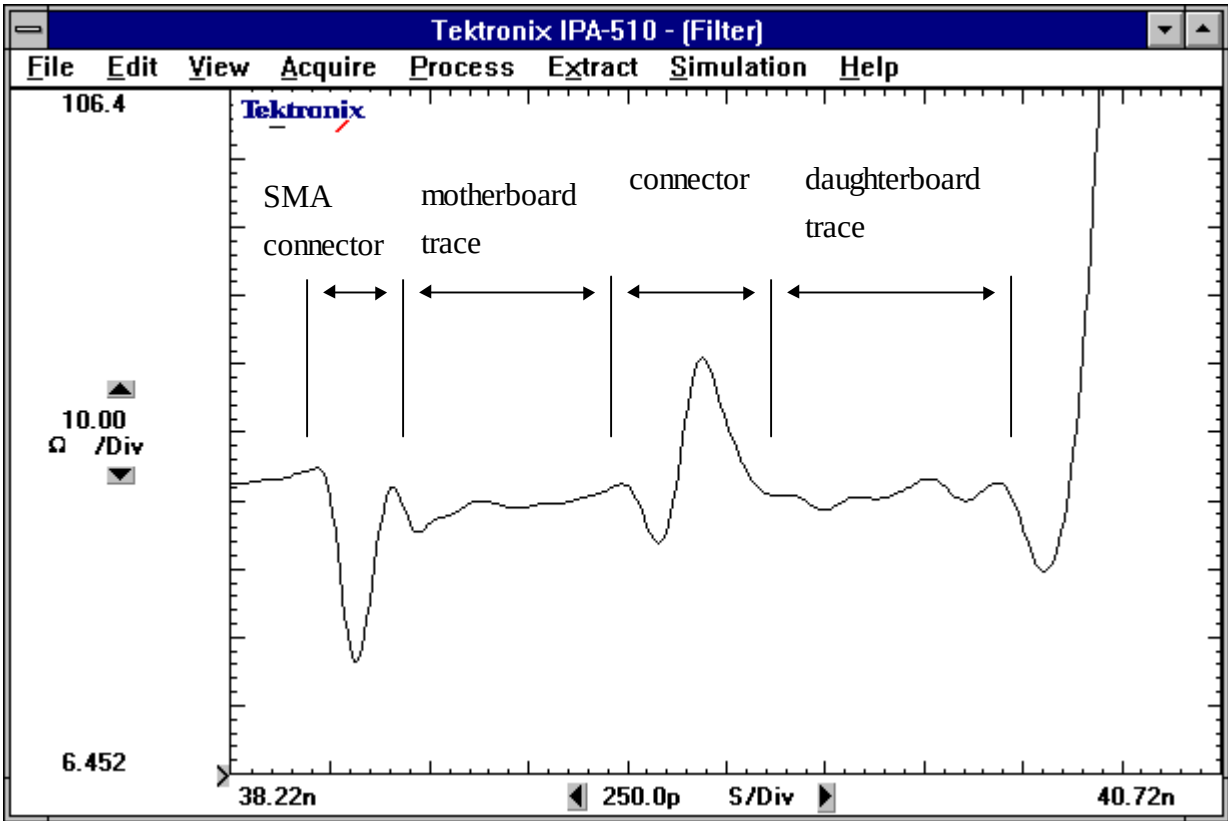


Figure D.1 – Example of an impedance profile of connector using a measurement system rise time of 35 ps

D.2 Effects of using variable rise times

Figure D.2 demonstrates the effects of using variable rise times (this plot was generated using software filters). As shown in the top TDR impedance trace (measured at a measurement system rise time of 35 ps), the impedance values vary greatly compared to the lower trace (measured at a measurement system rise time of 1 ns). This is due to the additional resolution that is provided by using the faster measurement system rise time.

NOTE — The variable rise time annex describes a number of methods by which the effective signal rise time may be varied.

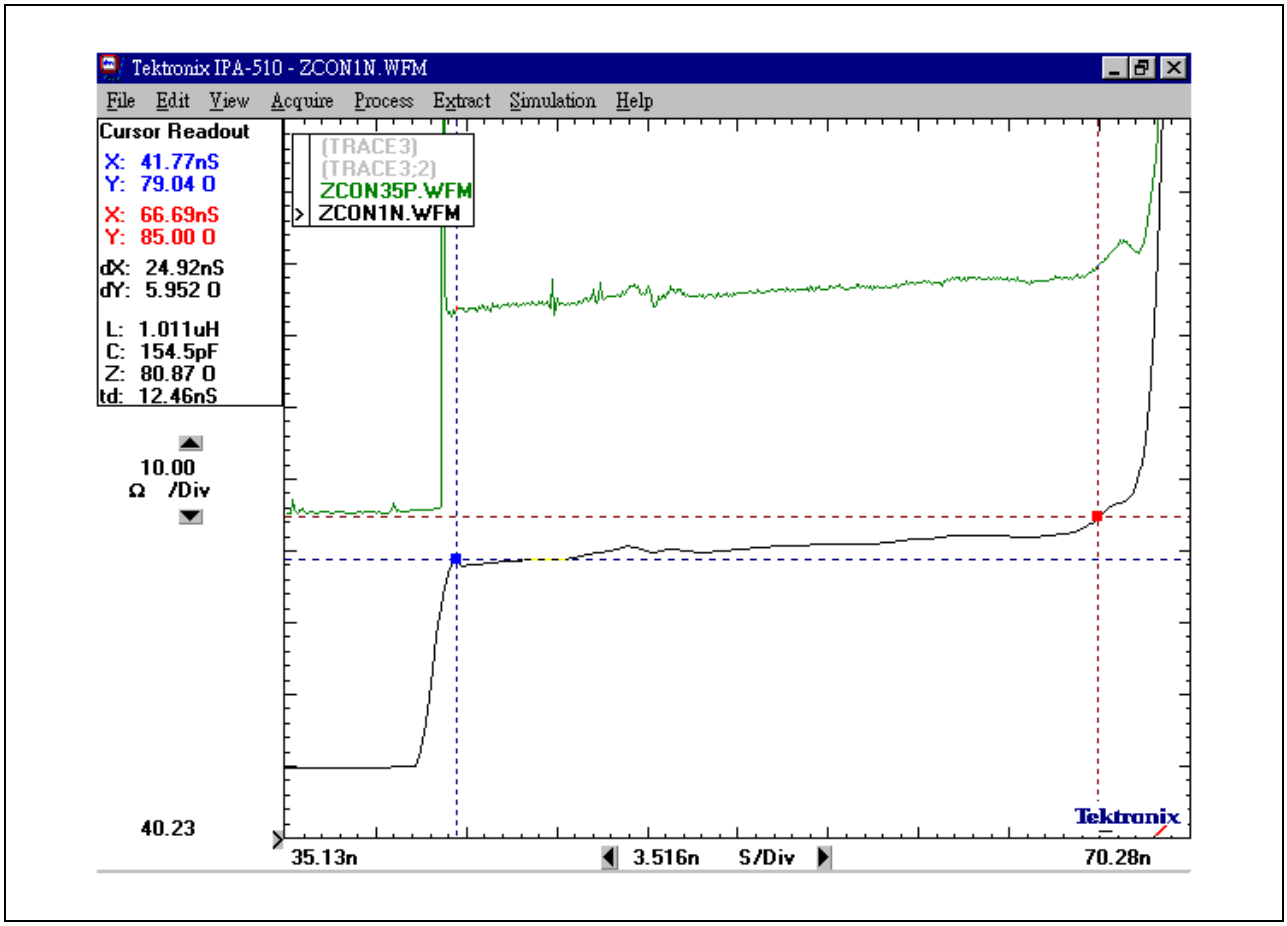


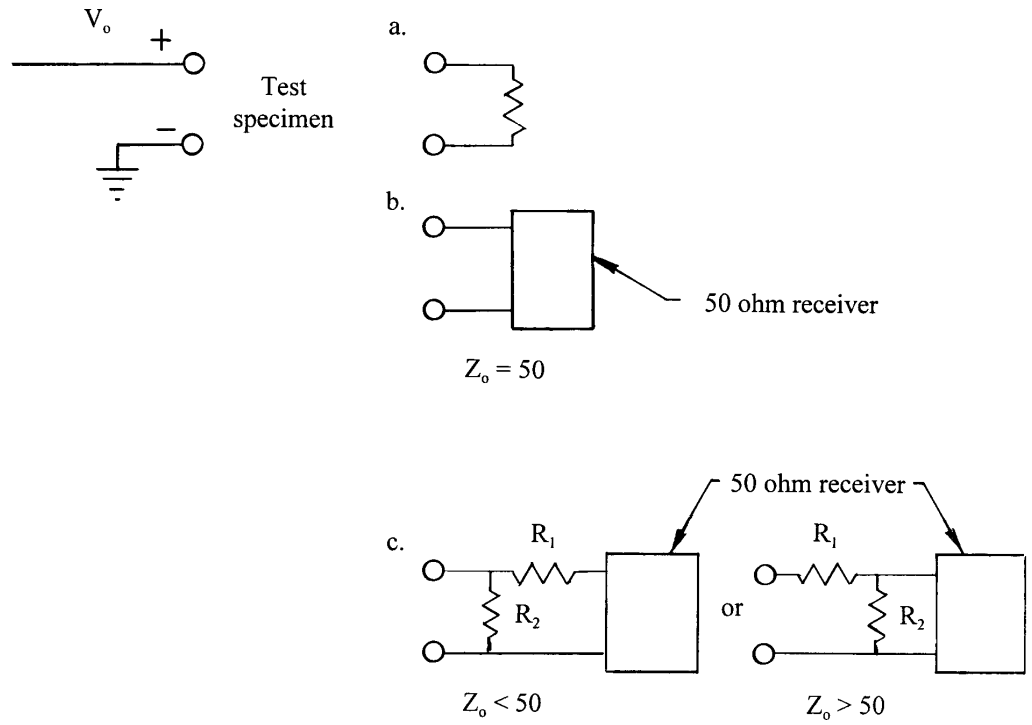
Figure D.2 – Example of impedance profiles of cable under the rise time of 35 ps and 1 ns

Annex E

E Terminations - electrical (informative)

E.1 When specified in the referencing document the fixture should allow measurements to be made with a resistive termination attached to the far end of the driven line, see figures E.1 and E.2. In order to reduce any extraneous reflections, it is also recommended that resistive terminations be connected to both near and far ends of any other specimen signal lines which may be strongly coupled electrically to the signal line being measured. Most instruments used for these measurements are internally terminated in 50 ohms or 75 ohms single ended at both source and receiver ports.

E.2 Perfect resistive terminations of the signal lines may not be possible at high frequencies due to parasitic reactances in both signal and ground conductors. These reactances will have an impact on measured results. In this case it is desirable that the test fixture duplicate the exact geometry (parasitics) of the actual application.

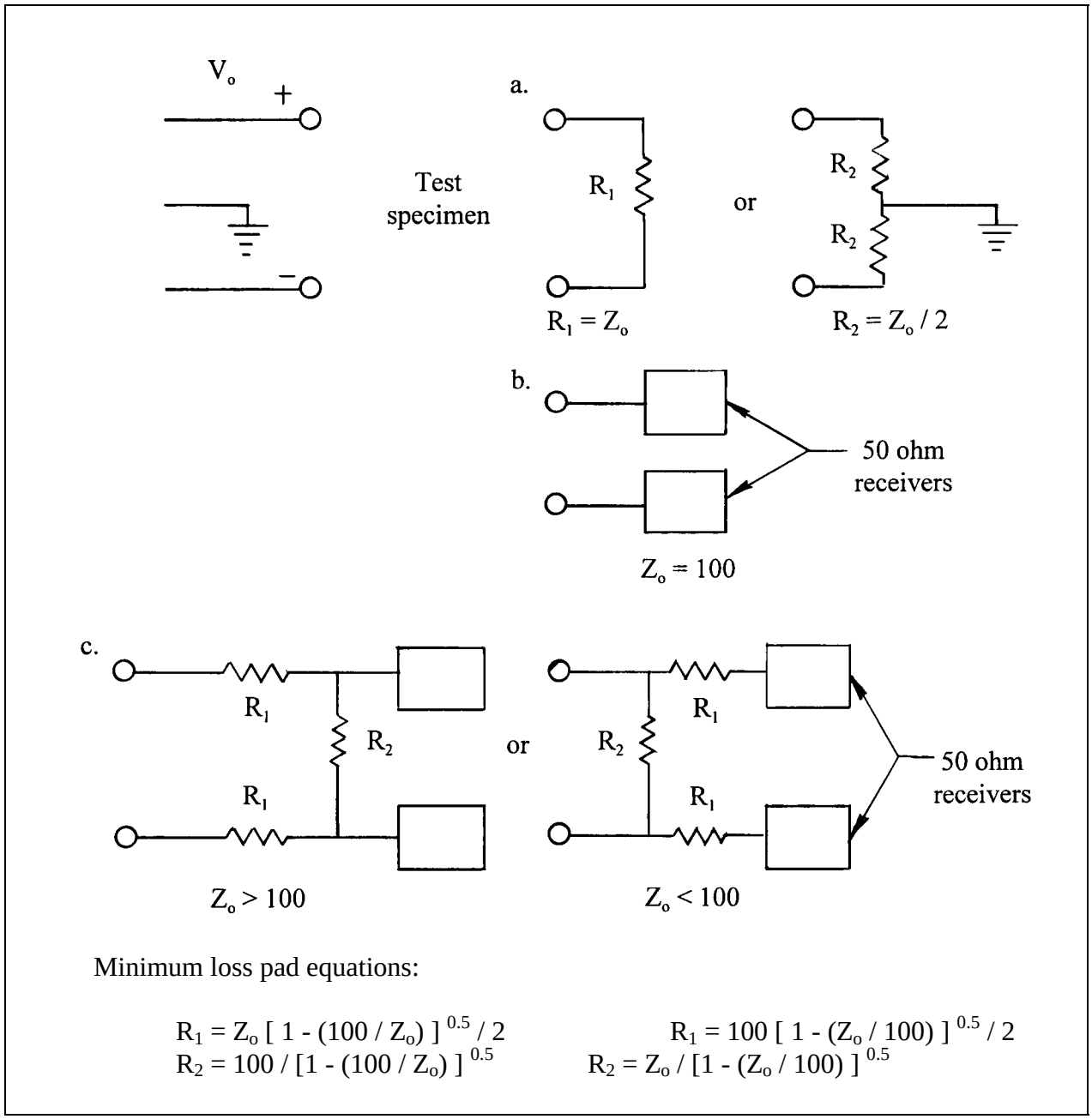


Minimum loss pad equations:

$R_1 = 50 [1 - (Z_o / 50)]^{0.5}$ $\quad$ $R_1 = Z_o [1 - (50 / Z_o)]^{0.5}$

$R_2 = Z_o / [1 - (Z_o / 50)]^{0.5}$ $\quad$ $R_2 = 50 / [1 - (50 / Z_o)]^{0.5}$

Figure E.1 - Single-ended terminations



Minimum loss pad equations:

$R_1 = Z_o [1 - (100 / Z_o)]^{0.5} / 2$
$R_2 = 100 / [1 - (100 / Z_o)]^{0.5}$

$R_1 = 100 [1 - (Z_o / 100)]^{0.5} / 2$
$R_2 = Z_o / [1 - (Z_o / 100)]^{0.5}$

Figure E.2 - Differential (balanced) terminations

Annex F

F Practical guidance - variable rise time (informative)

F.1 Many times it is useful to provide high speed electrical performance data at more rise times than just the unaltered rise time of the test equipment. For example, in the case of a TDR step, the rise time may be well below 100 ps, and different application rise times may be anywhere from 2 to 10 times that or even greater. As the fastest possible rise time has its merit as to the information it provides, it is also beneficial to understand how the interconnect system performs at the specific rise times of the applications that it will be used in.

F.2 As the technology within the test equipment becomes more advanced, many of the techniques can be handled within the test equipment itself, however if not available inside the test equipment, other methods do exist. These methods include, but are not limited to:

- Use of a step generator with the desired rise time
- Use of a faster step generator and a hardware filter
- Signal processing software within the test equipment
- Signal processing software external to the test equipment
- Frequency domain measurement converted to the time domain by digital signal processing (inverse Fourier transform)
- No method used (i.e. only the unmodified TDR/TDT rise time is used.)

NOTE — The test professional should be aware of all filtering which modifies the rise time within a test system. This includes not only the methods listed above but also cables, printed circuit board traces, connectors, etc. Each of these fixture components are necessary in the fixture test circuit, however they do have an effect on the rise time and should be measured and understood as to what the total effective measurement system rise time is.

Annex G

G Printed circuit board design considerations for electronics measurements (informative)

G.1 The designer should take precautions in designing printed-circuit boards for high-speed testing for several reasons. These include reflections due to impedance mismatches, signal attenuation due to skin effect of the narrow conductors, resonance effects due to long traces, crosstalk between traces, and others. Printed circuit board features that may be of concern include vias, SMT pads, probe interface, etc. Electrical discontinuities caused by these features are unavoidable in the test fixture(s), and shall not be overlooked as they may affect the impedance results of the specimen. This annex can not in the space allotted cover these topics in detail, but will attempt to lay the groundwork for further analysis and design, and refer the reader to more detailed treatments of the subject. There are a number of excellent references on the subject, which are listed at the end of this annex.

G.2 When the printed circuit board traces approach critical lengths (defined later in the document), it becomes essential to design the traces to match the impedance of the test equipment to avoid inaccurate results due to reflections. Controlling the line impedance of Printed circuit board traces is difficult without the use of embedded reference planes in the board. The preferred reference plane is one connected to signal ground, but any low impedance reference will work (including a voltage plane) if it is sufficiently decoupled. The signal line impedance is determined by conductor geometry, including the trace width and thickness, distance from the ground or other reference plane or conductor, and the dielectric constant of the board material. In the case of differential trace pairs, the spacing between the two traces is also critical. Several formulas exist for calculation of printed circuit board trace impedance, and a number of impedance calculation software tools are also available. The choice of board impedance formula is based on the conductors' relative placement as well as their position in the board cross-section, some common examples of which are shown in the figures below.

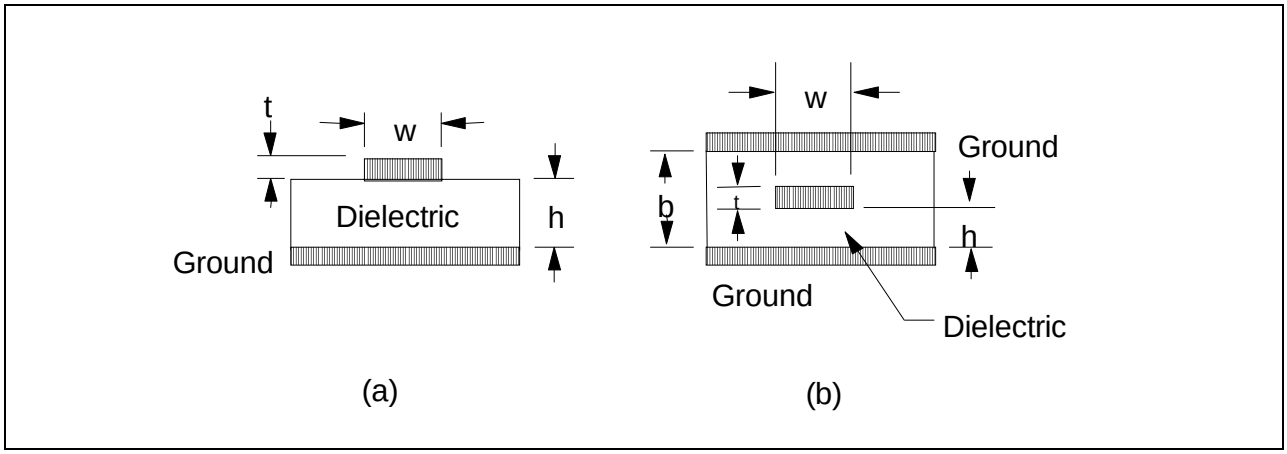


Figure G.1 - Microstrip (a) and stripline (b) geometries

G.2.1 In figure G.1(a), a cross section of a microstrip transmission line is shown. The signal line of width *w* and thickness *t* lies on top of the surface of the dielectric layer with relative dielectric constant ε_r (typically between 4 and 5 for glass-epoxy boards) at a height of *h* above a ground or other reference plane. The characteristic impedance of a signal line with such a structure is given by the following equation. [1)]

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r} + 1.41} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

G.2.2 This value is approximate, in that it assumes that the conductor is surrounded on three sides by air; if the conductor is covered by solder mask or other material (as is typical), the higher dielectric constant of that material will lower the impedance from the value calculated using the equation.

G.2.3 The stripline structure shown in figure G.1(b) is one in which the signal line is surrounded by the dielectric material, with ground or reference planes on two sides. The characteristic impedance for the stripline structure is given by the following equation. [2)]

$$Z_0 = \frac{60}{\varepsilon_r} \ln\left(\frac{4b}{0.67\pi w\left(0.8 + \frac{t}{w}\right)}\right)$$

G.2.4 A similar structure also exists where the conductor in question is inside the surface of the printed circuit board but is only adjacent to a ground or reference plane in one direction. This is referred to variously as “buried” microstrip or “covered” microstrip, and is shown in figure G.2.

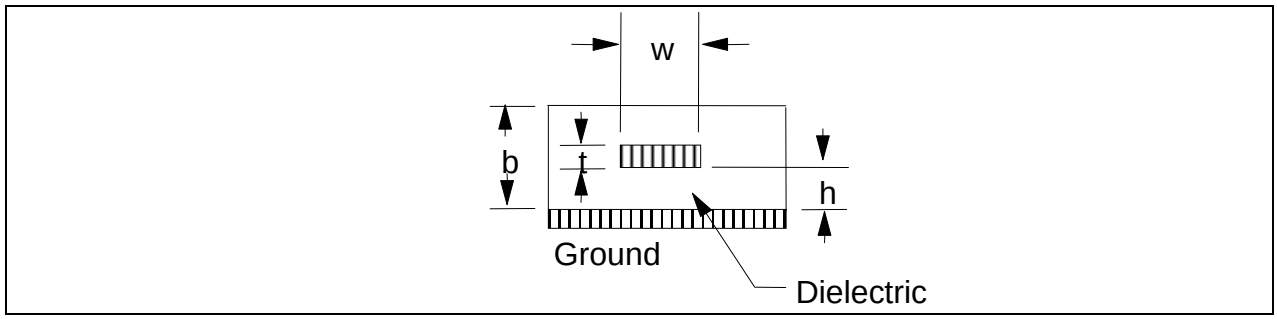


Figure G.2 - Buried microstrip geometry

1) Blood, William R., Jr.: MECL System Design Handbook (Phoenix, AZ: Motorola Semiconductor Products, Inc., 1988), p. 45.

2) Op. cit., p. 48.

G.2.4.1 The characteristic impedance for this configuration is given by the following equation. [3]

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

G.2.5 The equations above have all dealt with single-ended (unbalanced) signal lines. In the case of differential (balanced) signals, the impedance is more difficult to compute than the conventional single-ended impedance; the use of field solver software is often necessary to solve this type of problem. The use of vias is to be discouraged where possible, as the capacitance of vias causes impedance mismatches and consequent reflections in the signal path. In the event that surface ground planes are used to construct stripline structures, the surface and buried Ground planes should be connected together by vias spaced no more than $\lambda/8$ apart, to prevent resonances and other undesired effects on the printed circuit board.

G.2.6 Attenuation of high frequency signals (or higher order harmonics of non-sinusoidal signals) due to the so-called skin effect is a well-known phenomenon. Skin effect becomes significant when the skin depth δ is less than approximately one third of the conductor thickness. [4] The skin depth in meters at a given frequency of interest is given by $d = 0.0660/f^{½}$ [5], or approximately 2.1 mm at 1 GHz. Assuming 0.0014" thick (1.4 mils or 0.036 mm, commonly referred to as "one ounce" copper) conductors typically used for printed circuit board trace, this would indicate that skin effect would be significant at frequencies above approximately 85 MHz.

G.2.7 Another effect that should be considered is resonance. Resonance can cause unexpected results, and even oscillations in the device/fixture. This effect is not just manifested at the frequencies of the exciting signals, but also at harmonics of those frequencies present in the exciting signal; the spectral content of square or nearly square pulses can extend far beyond the expected maximum frequency. The maximum frequency of significant spectral content can be estimated *as* $f_{max} = 1/\pi t_r$, where t_r is the rise or fall time of the exciting signal. [6]

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3) Buchanan, James E.: BiCMOS/CMOS Systems Design (New York: McGraw-Hill, 1991), op. cit., p. 109.

4) Deutsch, A.: "Electrical Characteristics of Interconnections for High-Performance Systems," Proceedings of the IEEE, vol. 86, no. 2, February, 1998.

5) Ramo, S., Whinnery, J. R., and Van Duzer, T.: Fields and Waves in Communications Electronics (New York: Wiley, 1969), p.289.

6) Ott, Henry W.: Noise Reduction Techniques in Electronic Systems (NewYork: Wiley, 1976), p. 111.

NOTE — This is independent of the period of the signal. So, for a 100 MHz signal with a rise time of 1 ns, significant spectral energy exists in that signal up to approximately 300 MHz. The "critical length" at which a printed circuit board trace may cause problems due to resonance effects is given by the following equation. [7)]

$$l_{crit} = \frac{t_r}{2t_{pd}}$$

where:

t_r is the rise time of the signal and t_{pd} is the propagation delay per unit length in the medium (in the typical case, glass-epoxy). This propagation delay is typically 80ps/cm - 100 ps/cm (200 ps/in - 250 ps/in) on inside planes of printed circuit boards, and 55 ps/cm (170 ps/in) on outside planes, resulting in a critical length of approximately 6 cm (2 in) for a signal rise time of 1 ns.

G.2.8 The length to be used for calculating resonance is the wavelength of the frequency of interest in the medium, which is given by the following equation.

$$\lambda = \frac{v}{f}$$

where:

v is the velocity in the medium and f is the frequency of interest. The velocity in the medium is the reciprocal of the propagation delay, or approximately (1-2)x10^{10} cm/s (4-8x10^9 in/s), resulting in a wavelength of approximately 50 cm (20 in) at 300 MHz.

G.2.9 Crosstalk should be considered in the printed circuit board design, most obviously when designing a fixture for measurement of crosstalk, but also for others. The amount of crosstalk introduced is dependent on conductor geometry (width, spacing, and height above ground) as well as the coupling length, so it is difficult to give specific guidance. The reader is referred to [8)] for a discussion of the subject. A rule of thumb is that conductor spacing should be three times the conductor width to minimize crosstalk.

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

7) Buchanan, op. cit., p. 125.

8) Ibid., pp. 114-122.

G.2.10 Attention shall also be paid to the trace delay, especially when designing fixtures for measurement of propagation delay. Where trace length shall be added to equalize delay between paths on the fixture, sharp corners and serpentine wiring are not to be used. Sharp corners and serpentine wiring introduce impedance mismatches into the paths, and serpentine wiring changes the propagation delay per unit length due to the coupling between adjacent legs of the pattern. This will cause actual delays that are difficult to quantify.

G.2.11 General recommendations

- Unless otherwise specified all copper layers should be 1 ounce copper to minimize losses due to skin effect.

- Connect all ground pins to all ground planes.

- Vias connecting ground planes should be spaced no more than /8 apart. Filled vias are allowed.

- All signal traces on any style board (e.g. motherboard or daughter card) should be the same length.

- Traces should be separated (not running in parallel) as soon as possible upon escaping the connector footprint area to prevent crosstalk between traces.

  NOTE — Differential pairs should be routed as pairs.

- The electrical length of the pc board traces should be as short as possible.

  NOTE — For time-domain reflection measurements the electrical length of the pc board traces should be at least 3 times the measurement system rise time to be able to distinguish the discontinuities of the test board connection from the DUT. When using through hole connectors (SMA, BNC, etc) the trace length may need to be longer than 3 times the measurement system rise time.

- The test professional should be aware of the ringing that will occur from the impedance mismatches in the test fixture.

Other excellent references on these subjects include:

Johnson, H. and Graham, M.: High-Speed Digital Design, a Handbook of Black Magic (Upper Saddle River, NJ: Prentice-Hall, 1993)

Matick, R. E.: Transmission Lines for Digital and Communications Networks (Piscataway, NJ: IEEE Press, 1995)

Annex H

H Test signal launch hardware (informative)

Typical hardware for launching signals into test fixtures are listed below, including the broad advantages and disadvantages of each type..

H.1 Semi-rigid coax

H.1.1 Advantages

- Ease of repeating measurements (easy to screw/unscrew precision coax cables)
- Repeatable measurements on the same sample
- Sample preparation is faster (no test board required)
- One of the least expensive kinds to purchase
- Suitable for high frequencies (~10 GHz-20 GHz)

H.1.2 Disadvantages

- Delicate – solder joint may break with handling
- May by limited by pitch, (due to the diameter of the coax)
- Impedance discontinuity at the solder joint
- May not represent the application environment

H.2 Handheld probes

H.2.1 Advantages

- Ease of performing the measurement
- Speed of measurement
- Low cost – probe is reusable on many measurement points

H.2.2 Disadvantages

- Circuit loading
- Measurement repeatability, due to movable probe and user experience
- Bandwidth limitations
- Impedance discontinuities may be significant
- Probe capacitance may be comparable to specimen
- Maintaining good ground connection difficult

H.3 Microprobes

H.3.1 Advantages:

- Higher bandwidth than handheld probe
- Less impedance discontinuity than handheld probe or SMA
- More repeatable measurements due to fixed ground spacing
- Calibration is possible with the matching standard
- Finer pin pitch than other probe types

H.3.2 Disadvantages

- High cost
- Delicate nature – probes break easily
- Test board is still required
- Repeated use can scratch, damage pads on test board
- Special calibration standards may be required
- Signal-to-ground spacing must be specified on purchase, and not variable
- Impossible to hand hold - positioning hardware is typically needed.

H.4 SMA attach (on board)

H.4.1 Through hole

H.4.1.1 Advantages

- More mechanically robust than probes on pads or semirigid
- More repeatable measurements than probes on pads
- Less expensive than microprobes
- Usable with commonly available test cables

H.4.1.2 Disadvantages

- More expensive than pads on board or semi-rigid
- Limited reuse
- Large impedance discontinuity due to large via and pad footprint
- Relatively large physical size

H.4.2 End launch

H.4.2.1 Advantages

- Same as through hole SMA (see above)
- Smaller impedance discontinuity than through hole SMA

H.4.2.2 Disadvantages

- Less mechanically robust than through hole SMA
- Limited board thickness options
- More expensive than pads on board or semi-rigid
- Limited reuse
- Relatively large physical size
- Shall be mounted on edge of board – can increase trace length and routing difficulty

H.5 Other coaxial connectors

H.5.1 SMB (note: typically 75 ohms, not 50 ohms)

H.5.1.1 Advantages

- Snap on – faster to attach than SMA
- More mechanically robust than probes on pads or semirigid
- More repeatable measurements than probes on pads
- Less expensive than microprobes

H.5.1.2 Disadvantages

- Less widely used – special test cables, etc. may be needed, and may be higher cost than SMA
- Lower bandwidth than SMA
- Relatively large physical size

H.5.2 MMCX

H.5.2.1 Advantages:

- Good electrical performance

H.5.2.2 Disadvantages

- Less widely used – test cables, etc. needed
- More expensive than SMA

H.5.3 BNC (not recommended for use above 500 MHz due to limited bandwidth)

H.6 Test cables

H.6.1 Semi-rigid

H.6.1.1 Advantages

- Higher bandwidth than flexible cables
- Lower cost than flexible cables

H.6.1.2 Disadvantages

- Less mechanically robust, (capable of fewer repeated bending motions)

H.6.2 Flexible

H.6.2.1 Advantages

- Variety of lengths, bandwidths and associated costs readily available
- Easy to adjust position of device under test
- Easier to reuse than semi-rigid

H.6.2.2 Disadvantages

- More expensive than semi-rigid

H.7 Baluns and other devices for differential measurements

Baluns and similar devices for differential measurements have well defined characteristics over a specified frequency range. It is recommended that test professionals carefully evaluate (and verify as necessary) the hardware's suitability for the desired measurements.

EIA Document Improvement Proposal

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